# MICROELECTRONICS PROCESSING: DIODE & RESISTOR FABRICATION

**Samuel B. Lee[1], Alex K. Spady[2]**

[1] Department of Mechanical Engineering, Cal Poly, San Luis Obispo, CA 93407
[2] Department of Biomedical Engineering, Cal Poly, San Luis Obispo, CA 93407

**The objective of this processing is to expound the processing of diode and resistor fabrication on a silicon wafer and the results of the processing performed in the Micro/Nano Fabrication lab during the Winter 2018 quarter. Ultimately, diodes were not successfully fabricated, but several metal thin film resistors and diffused resistors were fabricated. It was found that the diodes are acting as resistors and not diodes. There was a 0% yield for the diodes and 15%, 96%, and 97% yield for m, n, and p resistors, respectively. This conclusion was discovered by the linear relationship between voltage and current for the diodes. This report details the following: (i) the process of microfabricating diodes and microelectronics (ii) the calculations and parameters for certain processing steps performed (iii) the yield, results, and characteristics of the devices. For the first section, the steps and procedure used to fabricate microelectronics are explained as well as key parameters and equations in order to perform the aforementioned steps. The general processing steps performed include cleaning, growing oxides, spin coating, exposing photoresist, developing photoresist, etching, stripping resist, diffusing dopants, sputtering, and metrology steps (profilometry, 4-pt probe for sheet resistance, groove and staining, and prober/micromanipulator). The following section recounts the equipment and material utilized as well as the parameters used and found in the actual processing steps. The last section describes the results of the processing, including the yield of the devices, the characteristics of the diodes and resistors, and the characteristics of steps. It is hoped that this report will inform those who are interested in learning about microfabrication specifically not only how to fabricate diodes and resistors but also how to characterize them as well.**

## Table of Contents

# Introduction

## a. Motivation

The motivation and objectives for the processing and this processing report is to learn the fundamentals of microfabrication. As the case with many other real life topics, the theory and the application do not always coincide. In microfabrication, this discrepancy or tolerances between the theory and application that occurs has been a major area of study due to the rising demand of electronics and the burgeoning interest to fabricate more and fabricate smaller. One of the greatest challenges that microfabrication engenders a need to be able characterize features indiscernible to the naked eye. This processing provides only a glimpse to a much larger field of microfabrication design, fabrication, and characterization.

## b. Background

The following section provides information on the significance of microfabrication and also the major steps/procedure used in microfabrication. This by no means completely encompasses all the subject material. This background prepares enough information for the particular case of creating a single type of diode and several resistors, but many of the concepts can be carried over to other devices and applications.

### i. Microfabrication

Microfabrication pervades nearly all subject areas. Just about 5 decades ago, a single transistor was a feat in itself, but today, integrated circuits contain billions of transistors [1]. Because more functionality can be achieved in less space, microelectronics has been the fodder for the technological advancement. Automation, cellular devices, personal computers, medical diagnostics, medical equipment, and many more areas have progressed to improve productivity and overall the standard of living.

Microfabrication involves the fabrication of features/objects smaller than 100 μm. To put that into perspective, a human hair is about 100 μm and a red blood cell is 10 μm. Now, Intel produces chips 14 nm in node length [2].

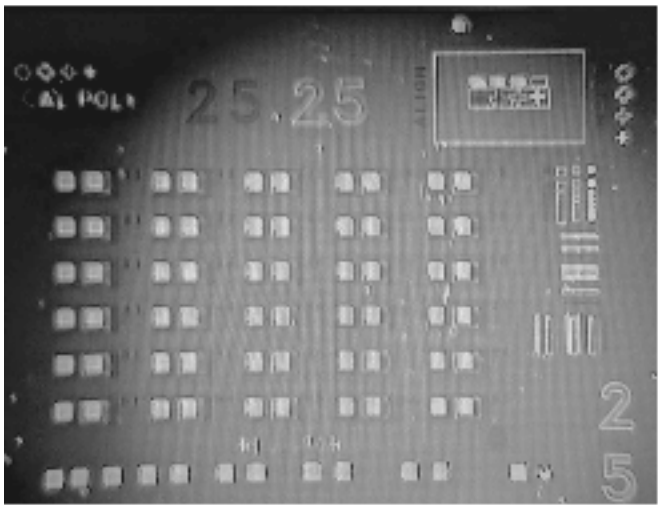



Figure 1. Image of part of a die (single instance of repeated device/feature) on a silicon wafer

Two fundamental components that make the building blocks for many microelectronics are diodes and resistors. Diodes can be thought the electrical equivalent to a hydraulic valve, particularly a check valve. The diode has two "biases" that the diode can be in, forward and reverse. In forward bias, the valve is open and flow of current is permitted. But, in reverse bias, the valve is closed and flow of current is not permitted.

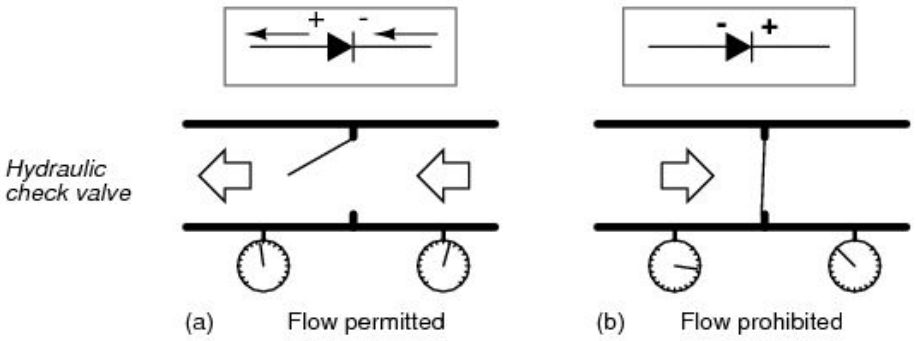



Figure 2. Circuit representation of a diode with the biase and the analogous representation to a hydraulic check valve [3]

It is important to note that diodes do have a limit on how long it can act as a closed circuit. There is a point called the breakdown voltage in which current starts to flow in the opposite direction that current flows in forward bias. Like check valves, they can only withstand a certain rated pressure before leakage or failure occurs.

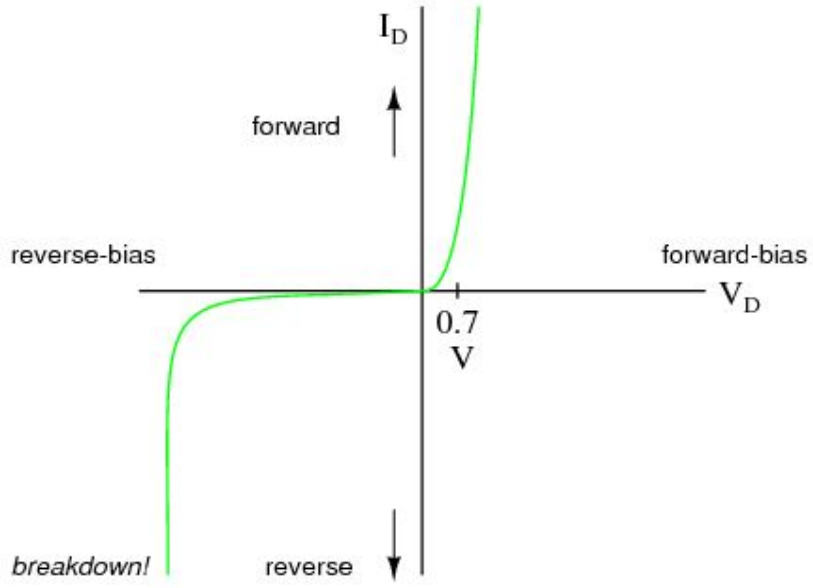
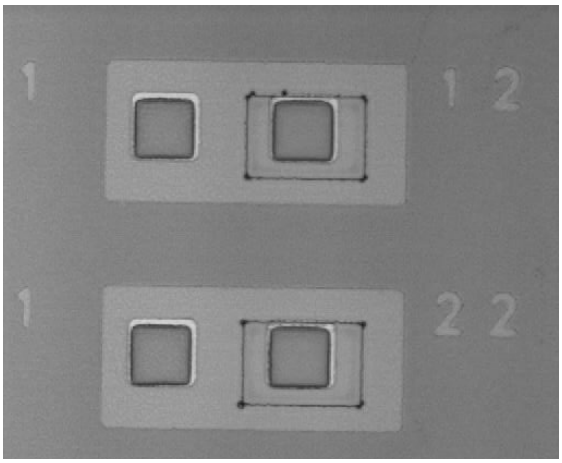


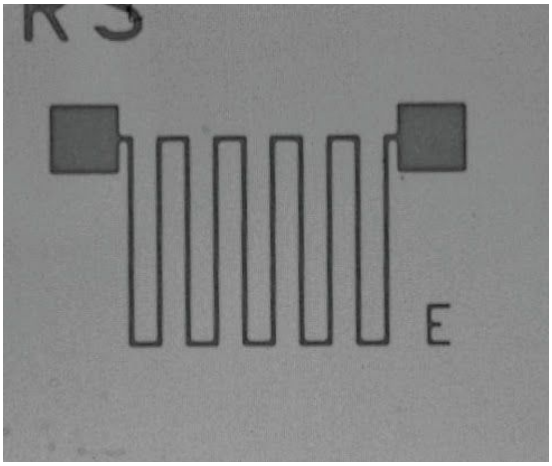

Figure 3. Current vs voltage of a diode to show the characteristics of forward and reverse bias [3]

The current and voltage plot shows that in forward bias, at a low voltage the current through the diode becomes practically infinite, or in other words, a short. In reverse bias however, for certain levels of voltage, the diode does not allow current, an open. The plot also shows that diodes do not have a linear current and voltage relationship.

After a certain voltage level in reverse bias, the diode breaks down and allows current to flow. Diodes are utilized in many applications from logic gates, metrology, power converters (rectifiers), and even in integrated circuits [3]. An example of a processed components are shown below.




(a) Diode




(b) Thin-film metal resistor

Figure 4. Top views of processed components

Next, another fundamental electrical component which is used in almost every circuit is a resistor. There are many kinds of resistors, but in microelectronics, the main types of resistors used are diffused, ion-implanted, thin-film, and polysilicon.

Table 1. Types of microelectronic resistors [4]

| Resistor Type | Fabrication | Advantages | Disadvantages |
|---|---|---|---|
| Diffused | Diffusing a dopant into silicon changes the resistivity, thereby changing the resistance | Economical and does not take up too much space | Sensitive to voltage |
| Ion-implanted | Ion-implanting a substance into a substrate | Resistor between layers; high resistances | More expensive and requires annealing |
| Thin-film | Evaporation or physical vapor deposition of a thin-film | High precision and stability | Requires several processing steps; costly |
| Polysilicon | Depositing a film of polysilicon and then | High values of resistance | Several processing steps; wide tolerances |

Resistors have many applications such as distributing/controlling current, dividing voltages, creating transistors, timing, and heating [5].

## ii. Major Processing Steps

In order to create these diodes, resistors, and etc, there are some major processes involved. The processes included here are only some of the unit processes that form microfabrication. Furthermore, new research continuous develops new and better techniques. The table shown in the next page is more specific to the diode and resistor

processing, but, as mentioned at the beginning of the background, many of the basics carry over to other devices/applications.

In general, microfabrication starts with the growth or purchase of a silicon wafer. Then, many of the steps occur in a clean room, a special lab where air is constantly filtered and only a certain amount of contaminants are allowed in. Afterwards, many of the steps involve adding, growing, and removing material. In order to make features, several methods are used to pattern geometry onto the wafer such as lithography, using light and a light sensitive substance called photoresist to pattern.

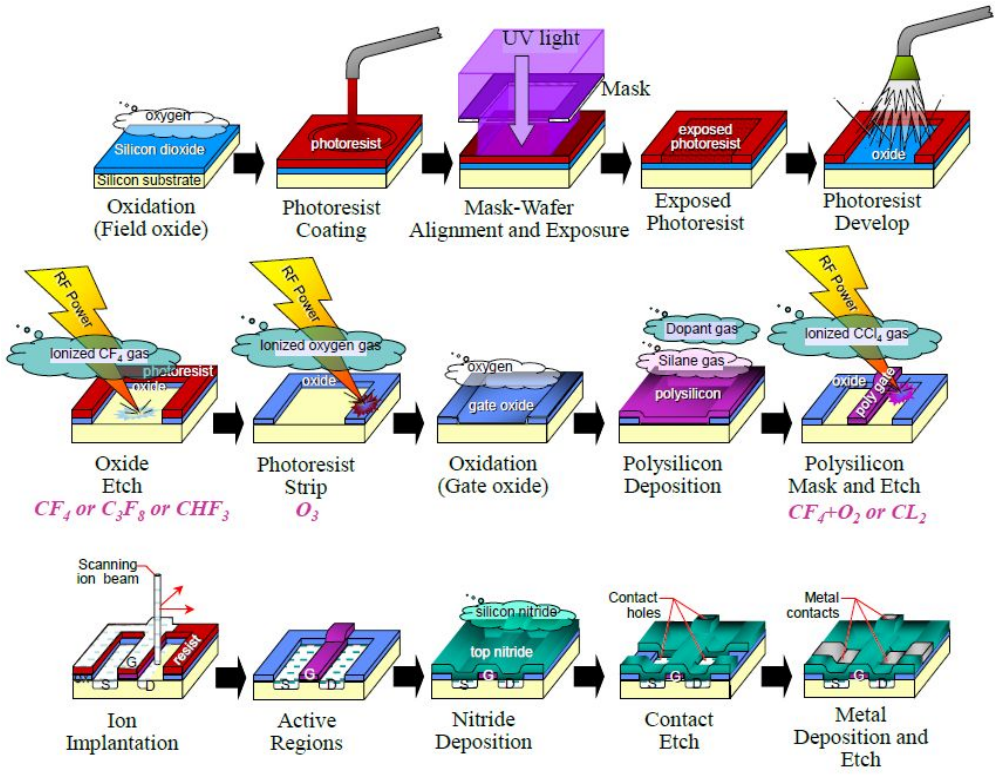



Figure 6. Major microfabrication processes schematic example of a transistor [7]

This is an example of the different steps and processes in microfabrication.

Table 2. Processes in microelectronics

| Step | Purpose | Parameters |
|---|---|---|
| Cleaning | Cleaning the wafers via immersion in solvents or blowing with gas is crucial for keeping particulates off of the wafer surface. | Solvents, solvent temperature, immersion time |
| Oxidation | Conversion of silicone into silicone dioxide to act as a mask or insulator. | Type (wet or dry), oven orientation (horizontal or vertical), oven temperature, time in oven, wafer placement |
| Spin coating | Obtain a homogeneous layer of light-sensitive photoresist based on a predetermined target thickness. | Spin speed, spin time, photoresist density and viscosity, soft bake temp, soft bake time, dispensed resist amount |
| Soft Bake | Drive off excess photoresist solvent. | Hot plate temp, soft bake time |
| Expose | High intensity light source is used to induce chemical change in the photoresist, making uncovered portions insoluble or soluble. A mask is used to expose only the necessary areas. | Aligner energy density, exposure dose, exposure time |
| Post-Exposure Bake | Reduces standing wave profile caused by constructive and destructive interference from incident light [6]. | Hot plate temp, time on hot plate. |
| Develop | Developer removes all soluble photoresist. | Developer chemical used, immersion time |
| Hard Bake | Stabilize and harden the developed photoresist prior to further use. | Hot plate temp, hard bake time |
| Etch | A precalculated etch rate is used to remove wafer substrate from areas not covered by photoresist. | Type (wet or dry), etch material, etchant, etch profile (isotropic or anisotropic), etch time |
| Strip | Chemically removes resist from the substrate surface. | Resist strip solution type, solution temperature, time in solution, resist type (pos or neg). |
| Diffusion | Diffuse dopant of choice into your substrate at a certain depth. | Wafer order, furnace temp, bake time, oxygen gas flow rate, loading speed, desired junction depth, type of dopant. |
| Sputtering | Method used to deposit material from a target source onto a wafer substrate. | Target thickness, base pressure, sputter time. |

Some other processes that are involved include is not limited to ion-implantation, rapid thermal processing (RTP), annealing, chemical vapor deposition (CVD), chemical-mechanical planarization (CMP), evaporation, reactive ion etching (RIE), dicing, and wire-bonding. For more information on these processes, refer to a microfabrication resource such as *Fabrication Engineering at the Micro- and Nanoscale* by Stephen A. Campbell [1].

Another important aspect to microfabrication is not just the design and fabrication but also the characterization and testing of the finished components. Testing is required to find whether the components perform and perform as expected/desired. Testing occurs not just at the end but also during the processing as well for a couple reasons.

One, it demonstrates whether the processing is going correctly. Two, it helps determine quality issues such as steps in which many wafers fail and require to be reworked or, worst case, completely thrown out. Some of the major metrology tools are used to measure resistance, junction depths from depths, film thicknesses, and imaging (microscopes).

# Materials and Methods

This section describes the actual equipment/materials used, procedure that was followed for processing, and the parameters used for the steps with the calculations required to acquire those

## a. Equipment Used

The silicon wafers used for the processing were P-type (100) 100 mm diameter from Ultrasil. For the processing of the diodes and resistors, the following equipment was used.

Table 3. Equipment used for major processes

| Step | Equipment | Chemicals/Substances |
|---|---|---|
| Cleaning | SEMITOOL PSC-101 SRD | Piranha (H2SO4 : H2O2 (9:1));<br>BOE (Buffered oxide etch) |
| Oxidation | STT-1200C-6-12 | $O_2$, $H_2O$, and $N_2$ |
| Spin coating | Laurell WS-400BZ-6NPP/LTE | Boron dopant (Filmtronics: B155)<br>Phosphorus dopant (Filmtronics: P507)<br>Shipley S1813 positive photoresist |
| Expose | GAMM (Quintel) Aligner | N/A |
| Develop | N/A | Microposit CD-26 |
| Diffusion | STT-1200C-6-12 | $O_2$ and $N_2$ |
| Etch | N/A | BOE<br>Transene Aluminum Etchant Type A |
| Sputtering | Rohwedder sputtering system | Argon |

Other equipment was used for metrology both during and after the processing.

Table 4. Metrology equipment*

| Equipment | Metrology Purpose |
|---|---|
| Digital drop gage | Wafer thickness |
| S-301 4-pt Probe | Sheet resistance |
| Filmetrics F20 | Film thickness |
| Signatone 1100 | Junction depth |
| Prober (microscope, micromanipulators, and multimeter) | Resistance, current |
| Microscope | Optical inspection |

*For a more complete listing of the equipment, see Appendix A: Equipment.

## b. Summary of Process Sequence

In order to fabricate the diodes and resistors, the following sequence was used.

Table 5. Simplified summary of process sequence

| Step # | Step in Full Sequence | Process |
|---|---|---|
| 1 | 1 | Wafer selection |
| 2 | 2 | Scribe wafers |
| 3 | 4 | Clean |
| 4 | 3,5 | Initial metrology (thickness; SR) |
| 5 | 6-7 | Oxidation; grow diffusion mask 1 |
| 6 | 8-15 | Litho mask 1 |
| 7 | 16-22 | Diffusion 1 |
| 8 | 23 | Clean |
| 9 | 24-27 | Oxidation; grow diffusion mask 2 |
| 10 | 28-35 | Litho mask 2 |
| 11 | 36-45 | Diffusion 2 |
| 12 | 46 | Clean |
| 13 | 47-53 | Oxidation; grow field oxide |
| 14 | 54-60 | Litho mask 3 |
| 15 | 61 | Sputter aluminum |
| 16 | 62-63 | Sputter metrology (thickness; SR) |
| 17 | 64-69 | Litho mask 4 (*no cleaning) |
| 18 | 70-72 | Finished device metrology |

For the complete process process sequence, refer to Appendix B: Full Process Flow. Some of the steps such as oxidation, lithography steps, and diffusion are reduced.

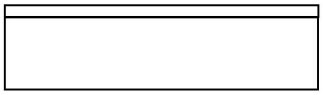
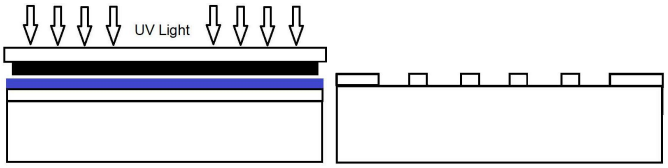
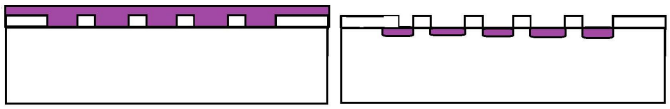
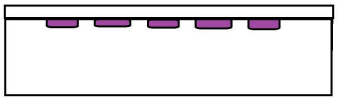
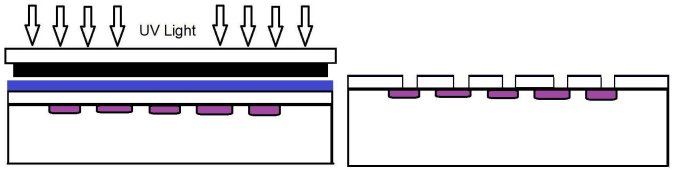
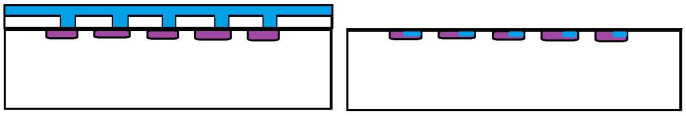
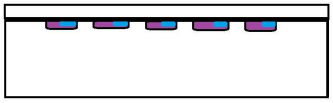
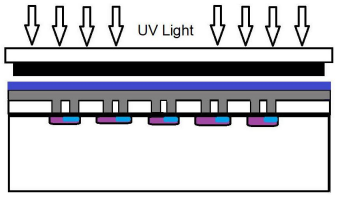
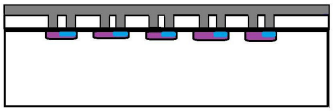
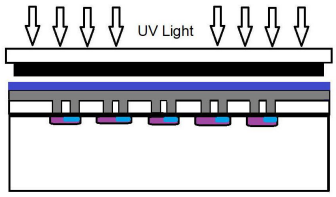
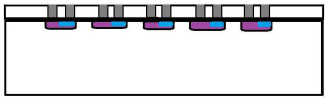
Table 6. Expanded steps of oxidation, lithography and diffusion

| Unit Process | Step # | Step Description |
|---|---|---|
| Oxidation | 1 | Oxidation; grow oxide |
| | 2 | Oxidation metrology (thickness; SR; G+S) |
| Lithography | 1 | Clean |
| | 2 | Spin coat resist |
| | 3 | Expose with mask |
| | 4 | Develop |
| | 5 | Measure etch rate |
| | 6 | Etch |
| | 7 | Strip resist |
| | 8 | Clean |
| Diffusion | 1 | Spin coat dopant |
| | 2 | Diffusion |
| | 3 | Diffusion mask thickness |
| | 4 | Etch off mask |
| | 5 | Diffusion metrology (SR; G+S) |

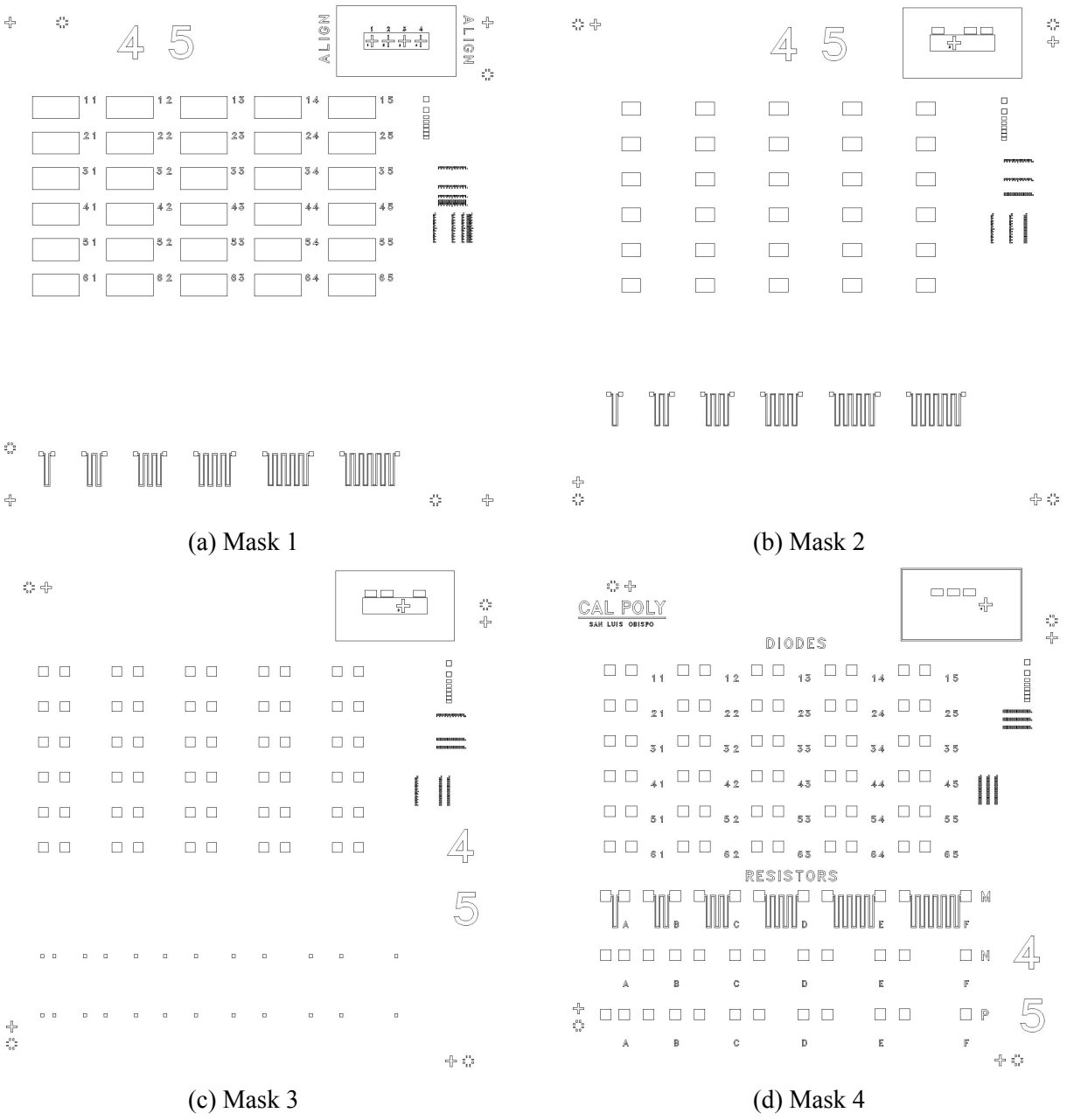
These steps show the typical process with microfabrication. Cleaning, growing material (oxide), patterning (litho), removing material (etching), and adding material (sputtering and diffusion). Further along the process more and more metrology steps are needed to characterize and see if the process is going as predicted and desired. Any steps that require high heat such as oxidation and diffusion usually add more metrology steps because high heat steps affect not just the surface and the current process but all those before as well.

To help visualize the steps that occur to make the diodes and resistors, the table in the following page provides a cross-sectional schematic of the major steps from the simplified summary of the process flow.

Table 7. Process sequence with schematic and images

| Step # | Process | Cross-sectional Schematic [8] |
|---|---|---|
| 5 | Oxidation; grow diffusion mask 1 |  |
| 6 | Litho mask 1 |  |
| 7 | Diffusion 1 |  |
| 9 | Oxidation; grow diffusion mask 2 |  |
| 10 | Litho mask 2 |  |
| 11 | Diffusion 2 |  |
| 13 | Oxidation; grow field oxide |  |
| 14 | Litho mask 3 |  |
| 15 | Sputter aluminum |  |
| 17 | Litho mask 4 (*no cleaning because aluminum reacts with Piranha) |  |
| 18 | Finished device metrology |  |

In order to pattern the resist and etch only certain of the wafers, a mask is used.




(a) Mask 1

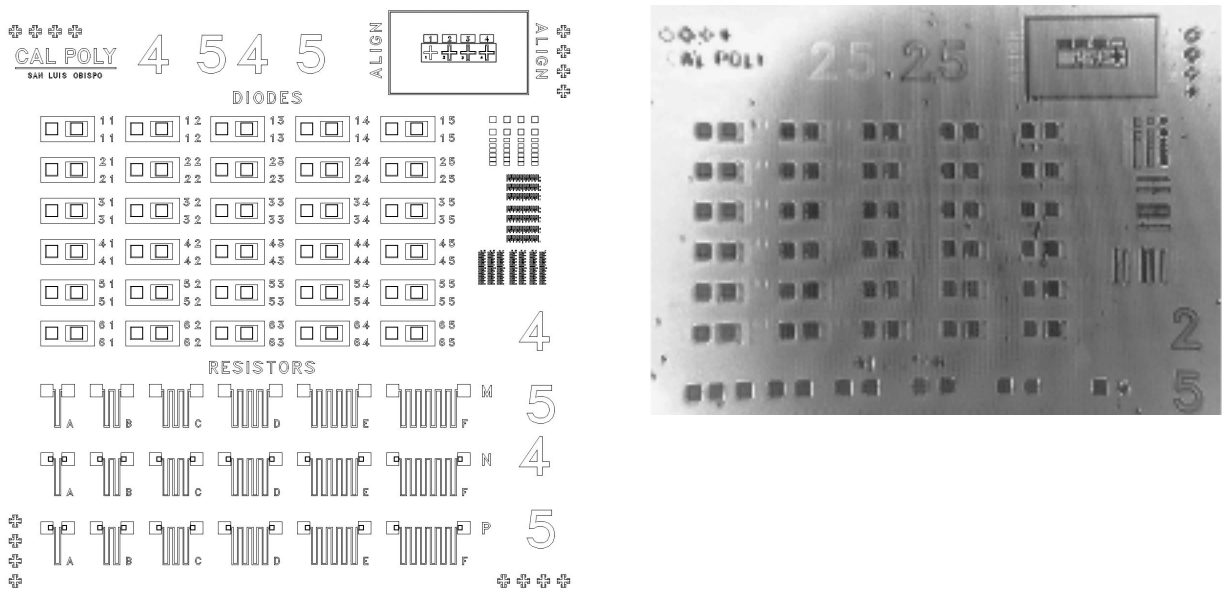
(b) Mask 2

(c) Mask 3

(d) Mask 4

Figure 7. Masks for photolithography. Mask 1 and 2 are used for the diffusions. Mask 3 is used to make the aluminum contacts. Mask 4 is to for etching the aluminum.

Each mask is used on the same wafer, and so features become overlayed on a wafer. The final overlay of all the masks looks similar to the final device.




(a) All masks (b) Processed die

Figure 8. Comparison between the mask and a finished die on a processed device wafer.

Though the focus on the processed die makes it hard to discern, it can be seen that the final die and mask are similar. The purpose of the numbers on the top and on the right are to keep track of each die on a single wafer. The top right corner and also every corner contains alignment marks that help make sure each layer is aligned. A larger image of the masks can be found in Appendix C.

During the processing, not all the wafers become finished components. To maintain a record of the steps for quality purposes, control wafers are processed along with the wafers that will later become devices. These control wafers have many purposes for example, one or several control wafers are used as an exposure matrix to find the optimum exposure dose. A total of 19 control wafers were used. For more information, see Appendix D.

## c. Parameters Used for Major Steps

### i. Cleaning

Wafers are cleaned in order to remove foreign particulates and also sometimes to remove native oxides.

Table 8. Cleaning procedure

| Step # | Step Description |
|---|---|
| 1 | Load wafers into Teflon cassette |
| 2 | Immerse in warm (≈70°C) Piranha* for about 10 min |
| 3 | Deionized (DI) water quench 4X's |
| 4** | Immerse in room-temp BOE (buffered oxide etch) and repeat step 3 |
| 5 | Spin, rinse, and dry (SRD) machine |

* Sulfuric acid ($H_2SO_4$) and hydrogen peroxide ($H_2O_2$)

** This step is only done for cleaning right before a oxide layer is about to be grown.

## ii. Oxidation

To grow an oxide, the following procedure was used.

Table 9. Oxidation procedure

| Step # | Step Description |
|---|---|
| 1 | Load wafers into a quartz boat |
| 2 | Ramp up oven to a loading temperature (900°C) |
| 3 | Turn on $N_2$ at 6 LPM and load the wafers slowly into the furnace |
| 4 | Ramp up to oxidation temperature (1100°C) |
| 5 | Turn on $H_2O$ heater |
| 6 | Turn on $O_2$ at 6 LPM for duration calculated |
| 7 | Turn off $O_2$ |
| 8 | $N_2$ for 20 minutes during ramp down for 20 minutes |
| 9 | Allow the furnace to cool down |

The Deal-Grove model (1) was used to calculate oxidation time ($t$) was calculated based off a target oxide thickness ($X$). The model uses predetermined rate constants ($a$, $b$) while also accounting for any oxide already present ($\tau$) [9].

$$t + \tau = (X^2/b) + [X/(b/a)] \quad (1)$$

Wafers were loaded into a quartz boat prior to their entrance into the oxidation furnace. The wafer loading order is an important parameter to account for the distribution of heat in the furnace. Wafers that are loaded into the quartz boat last and first typically grow nonuniform oxide layers. This effect can be seen with by a multicolored spot/ring that forms on the first and last wafers.

Table 10. Oxidation parameters

| Oxidation Step | Oven Time w/ $O_2$ [min] |
|---|---|
| Diffusion mask 1 | 40 |
| Diffusion mask 2 | 10 |
| Field oxide | 35 |

The target thickness of the oxide was determined by using a figure found in *Introduction to Microelectronics*. Based on the type of dopant and temperature of the oven, the required mask thickness can be found.

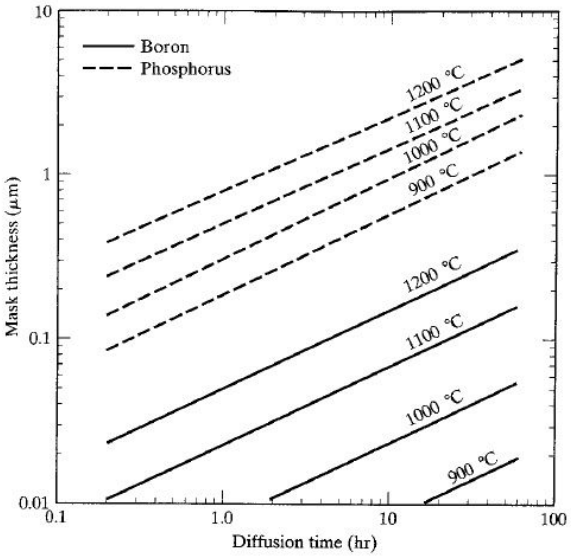



Figure 9. Wafer sectioning for oxide etch rate calculation [10].

## iii. Spin coating

Table 11. Spin coating procedure

| Step # | Step Description |
|---|---|
| 1 | Load HMDS primer, hexamethyldisilazane, for priming the wafer surface into a Eppendorf Pipette |
| 2 | Load resist into dispensing syringe |
| 3 | Program the spin coater to calculated parameters with spreading and planarizing steps |
| 4 | Load wafer onto vacuum chuck with centering tool |
| 5 | Spread and dry HMDS |
| 6 | Start the spin coater program |
| 7 | After the coating is finished, place the wafer onto a hot plate for a soft bake |

A thin layer of resist and dopant were applied to a wafer using spin coating. For each spin coat, there was a target thickness. In order to obtain that desired thickness, an equation was used (2) [11].

$$d = (4\rho\omega^2 t/(3\mu))^{-1/2} \quad (2)$$

Table 12. Spin coating parameters

| Spin Coat Step | Coat Substance | Spin Speed [rpm] | Spin Time [sec] | Dispensed Amount [ml] | Hot Plate Temp [℃] | Hot Plate Time [min] |
|---|---|---|---|---|---|---|
| Litho Mask 1 | Resist | 4000 | 20 | 5-6 | 115 | 2 |
| Diffusion Mask 1 | n-Dopant | 3000 | 10 | 3 | 200 | 5 |
| Litho Mask 2 | Resist | 4000 | 20 | 3-4 | 90 | 1 |
| Diffusion Mask 2 | p-Dopant | 3000 | 10 | 3 | 200 | 5 |
| Litho Mask 3* | Resist | - | - | - | - | - |
| Litho Mask 4* | Resist | - | - | - | - | - |

* No data was supplied on these process steps.

## iv. Expose resist

Table 13. Expose procedure

| Step # | Step Description |
|---|---|
| 1 | Turn on the aligner lamp including the vacuum and gases required |
| 2 | Load the mask |
| 3 | Set the exposure time |
| 4 | Load the wafer and follow the aligner instructions |
| 5 | Expose |
| 6 | Remove the wafer and transfer to developing |

Prior to use of the GAMM aligner, the exposure energy was measured. This, plus the manufacturer's stated target exposure dose for Shipley S1813 photoresist were used to determine an exposure time (3).

$$Dose = Exposure\ energy * Time * \%\ Transmitted \tag{3}$$

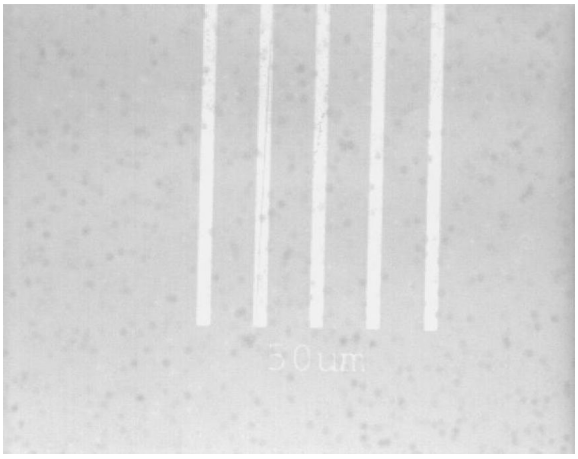
The exposure energy was found using a photometer. The % Transmitted is found by the amount of light that transmit through all the layers used to align the mask, i.e. any filters, support glass plates, and the transparency mask. For the processing, the % Transmitted was roughly estimated to be 63% based on light transmission through the layers used. Since the materials specify a recommended dose, the time of exposure can be found using Eq. 3. However, because the actual supplied dose can differ, an exposure matrix is done after developing to confirm and choose an exposure time based on a visual inspection.

## v. Develop resist

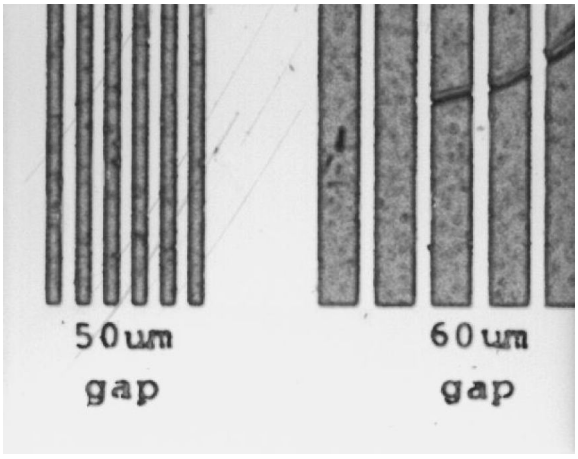
Table 14. Develop procedure

| Step # | Step Description |
|---|---|
| 1 | Load the wafers into a Teflon cassette |
| 2 | Immerse the wafers into a beaker with develop |
| 3 | After developing, dip in DI 4X's. Spin rinse and dry in SRD |
| 4 | Inspect wafers to qualitatively check for successful pattern transfer |
| 5 | Hard bake the wafers on hot plate at 150°C |

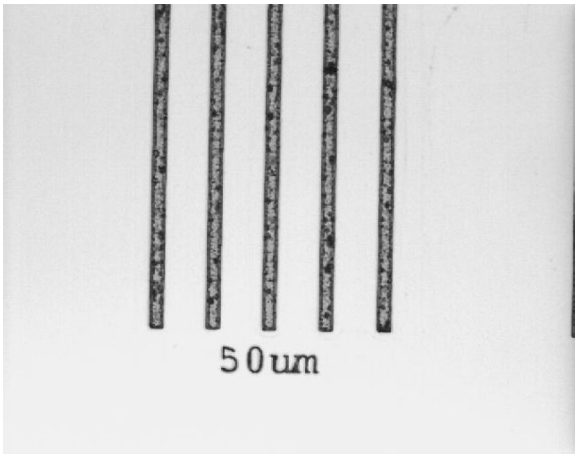
The developing stage of processing proved to be more qualitative than quantitative. The wafers were inspected post development to verify that the mask pattern had been successfully transferred into the resist. Images of individual wafer features were captured to assess for over development and underdevelopment. The exposure time was chosen based on a qualitative visual inspection.



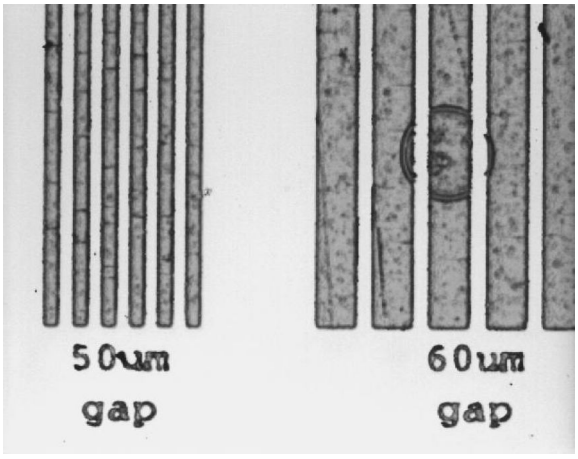

(a) Mask 1




(b) Exposed photoresist 25 seconds; chosen exposure time




(c) Exposed photoresist 20 seconds; underexposed




(d) Exposed photoresist 30 seconds; overexposed

Figure 10. Comparison of the mask and exposed photoresist for exposure time for diffusion mask 1

## vi. Etch

Table 15. Etching procedure

| Step # | Step Description |
|---|---|
| 1 | Load the wafers into a Teflon cassette |
| 2 | Immerse the wafers into the etchant and leave for calculated time |
| 3 | After etching, dip in DI 4X's. Spin rinse and dry in SRD |
| 4 | Transfer to strip resist |

The oxide etch rate was calculated by progressively lowering control wafers deeper into BOE at room temp. Each step lasted 60 seconds. The oxide thickness was then measured at each layer, and the average etch rate was determined using a plot of etched silicone dioxide over time. The wafer sectioning used to determine etch rate can be seen in Figure 11.

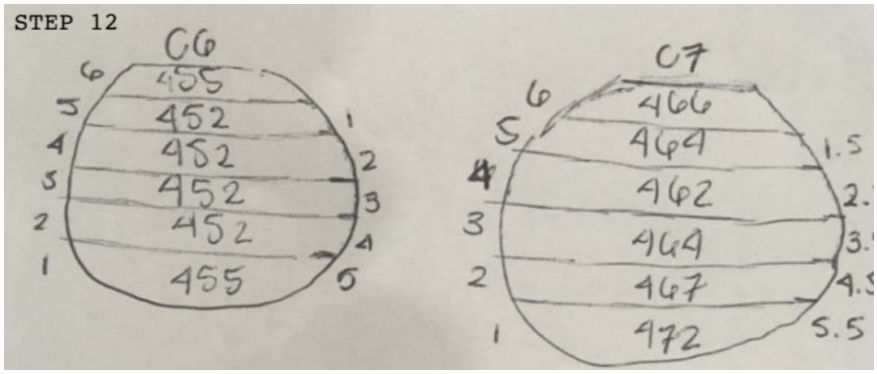



Figure 11. Wafer sectioning for oxide etch rate calculation.

The slope of oxide removed over time is the oxide etch rate, which can be found using a linear trend.

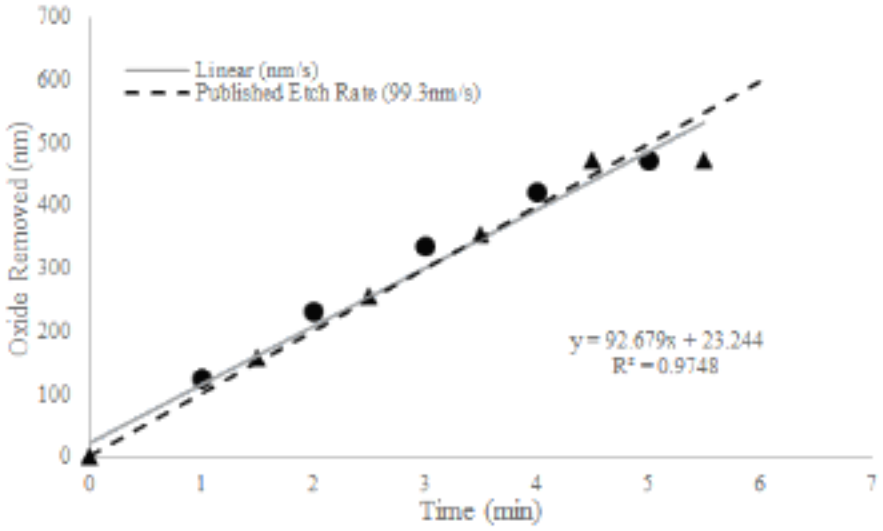



Figure 12. Oxide etch rate data (C8 and C7) compared to published value [12]

Now, for processing the actual device wafers, the etch time can be calculated using this equation.

$$Etch\ Time\ =\ Max\ Oxide\ Thickness\ \div\ Slowest\ Etch\ Rate \quad (4)$$

The maximum oxide thickness measurements from the oxide measurement step prior to etching was then used to calculate an etch time (4). Using the maximum oxide thickness and the slowest etch rate results in the longest etch time. The etch rate used in all the etch steps was 93 nm/s. Over-etching is preferred over under-etching because leaving an oxide prevents dopants from diffusing into the wafer. An additional 10% over-etch was included to account for any possibility of under-etch in the etch time.

### vii. Strip resist

Table 16. Resist strip procedure

| Step # | Step Description |
|---|---|
| 1 | Load the wafers into a Teflon cassette |
| 2 | Immerse the wafers into the stripper solution |
| 3 | Leave the wafers immersed for about 10 minutes |
| 4 | After etching, dip in DI 4X's. Spin rinse and dry in SRD |

The stripping solution was heated prior to submission of any wafers. Slight agitation of the solution once a minute is necessary for all resist to dissolve. The third resist strip, step 69, was not performed. Some wafers required to be stripped because of rework.

Table 17. Resist strip process parameters

| Strip Step | Solution Temp [℃] | Solution Vol [L] |
|---|---|---|
| Resist Strip 1 | 60 | 1.6 |
| Resist Strip 2 | 59 | 1.9 |
| Resist Strip 3 | - | - |

### viii. Diffusion

Table 18. Diffusion procedure

| Step # | Step Description |
|---|---|
| 1 | Load the wafers into a quartz boat |
| 2 | Ramp up oven to loading temperature (900°C) |
| 3 | Turn on $N_2$ at 6 LPM and load the wafers slowly into the furnace |
| 4 | Ramp up to oxidation temperature (1100°C) |
| 5 | Turn on $O_2$ at 6 LPM for duration calculated time |
| 6 | Switch $O_2$ to $N_2$ for 20 minutes during ramp down for 20 minutes |
| 7 | Allow the furnace to cool down |

Diffusivity (D) is a function of temperature (T), the activation energy ($E_a$) of the element being diffused, and a diffusion coefficient ($D_o$) which is based on lattice geometry [13].

$$D = D_o * exp(\frac{-E_a}{kT}) \quad (5)$$

Ultimately, diffusion of an element like boron into silicon is a two-step process requiring pre-deposition from a constant source, followed by drive-in at a constant dose. Junction depth ($X_j$) is found as a inverse error function involving the surface concentration, substrate concentration, specific diffusivity, and time (6).

$$D = 2\sqrt{D * t} * erfc^{-1}\ (\frac{C_{sub}}{C_{surf}}) \quad (6)$$

Table 19. Diffusion process parameters

| Diffusion Step | Oven Temp [℃] | Oven Time with $O_2$ [min] | $O_2$ Flowrate [LPM] |
|---|---|---|---|
| Diffusion 1 | 1100 | 60 | 6 |
| Diffusion 2 | 59 | 60 | 6 |

The order for wafers in the oven usually had the following order: dummy, controls, devices, controls, dummy. The dummies at the end were used to protect the other wafers from the ring/spot phenomenon mention in the intro of the diffusion step.

## ix. Sputtering

Table 20. Sputtering procedure

| Step # | Step Description |
|---|---|
| 1 | Check appropriate target is loaded |
| 2 | Check sputter power and rates |
| 3 | Load wafer |
| 4 | Pump chamber to about 200 mTorr |
| 5 | Set deposition pressure to 2.2 mTorr with argon |
| 6 | Set DC power to magnetron at 150 W |
| 7 | Sputter for calculated time |

For sputtering, the parameters changed for each wafer. Only one wafer can be sputtered at a time. Overall, the base pressure was about 1.5 x $10^{-6}$ mTorr, the pump down time of >1 hr, a sputter process pressure of 2-3 mTorr, and a sputter time of about 10 minutes. The target thickness was 400 nm.

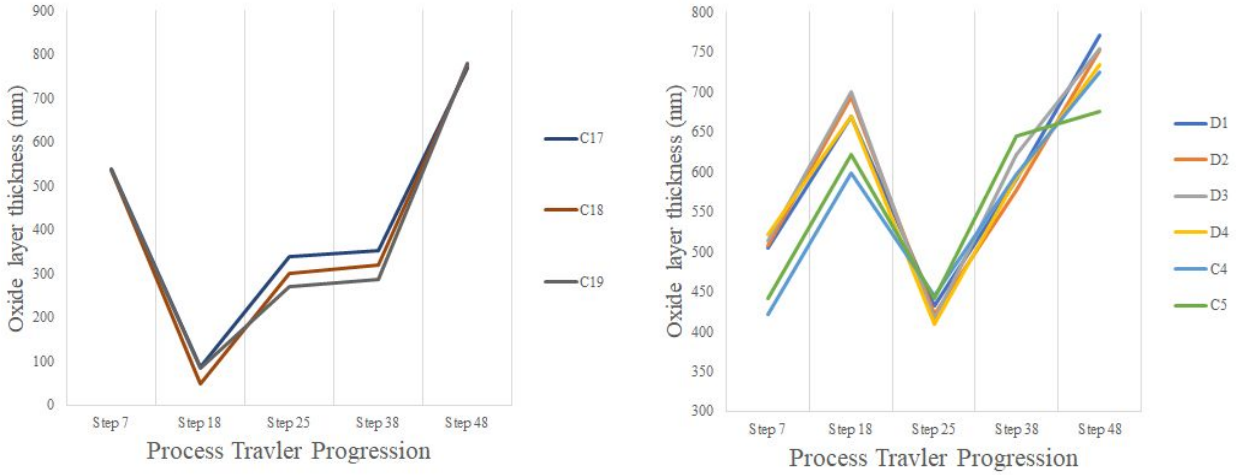
# Results and Discussion

## a. Processing Key Findings

During the processing, different metrology steps provided a history of the processing. This was done using three main metrology methods: interferometry for oxide thickness, groove and stain for junction depth, and 4-pt probe for sheet resistance. The data for

### i. Oxide Thicknesses

Oxide thickness measurements were taken at five timepoints throughout the diode fabrication sequence. All device wafers (D1-D4) plus five control wafers (C4, C5, C17-C19) were measured at each step. Various differing control wafers were also measure at these time points, this oxide thickness data can be seen in Appendix E.




(a) No dopant control wafers

(b) Doped wafers

Figure 13. Oxide thicknesses for wafers throughout processing.

Initial measurements conducted during step 7 confirmed that our device wafers had met the target thickness of 500nm . Plot a in figure 13 follows three control wafers without dopant throughout their processing sequence. The doped wafers proved to have thicker oxide layers throughout processing due to the higher density of defects in the doped wafers. Control wafers, C4 and C5, were below the 500 nm target thickness and confirmed that oxide thickness in a horizontal furnace is dependant on wafer position in the furnace as seen in Figure 14. The control wafers C17, C18, and C19 did not have this issue as they were placed near the back of the furnace. Figure 14 plots oxide thickness as a function of wafer position, showing that wafers near the entrance of the oxidation furnace grow substantially less of an oxide layer compared to those in the middle or near the end of the wafer boat. Device diodes are placed in the middle of the control wafers which serve as a buffer to ensure prime furnace position.

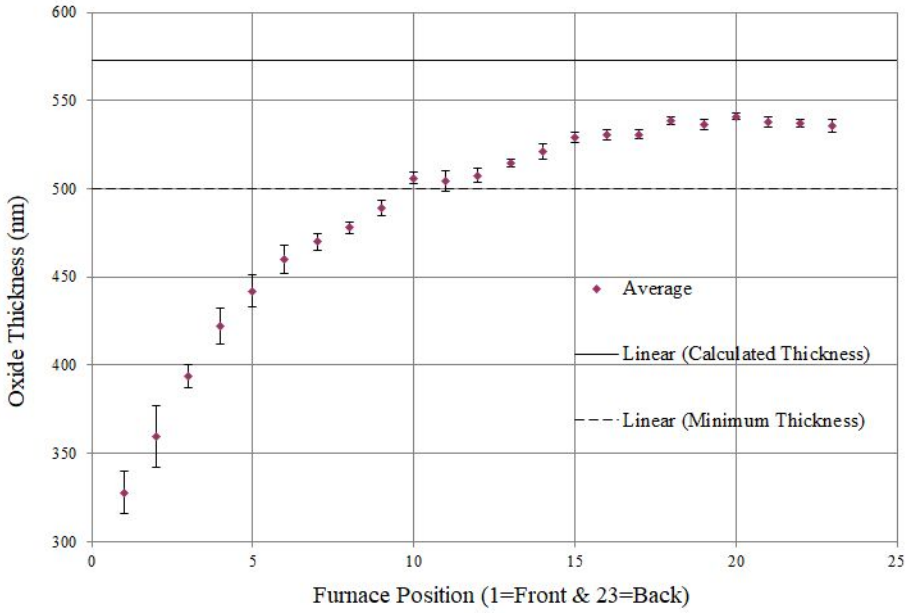



Figure 14. Oxide thickness change based on wafer position.

## ii. Junction Depth

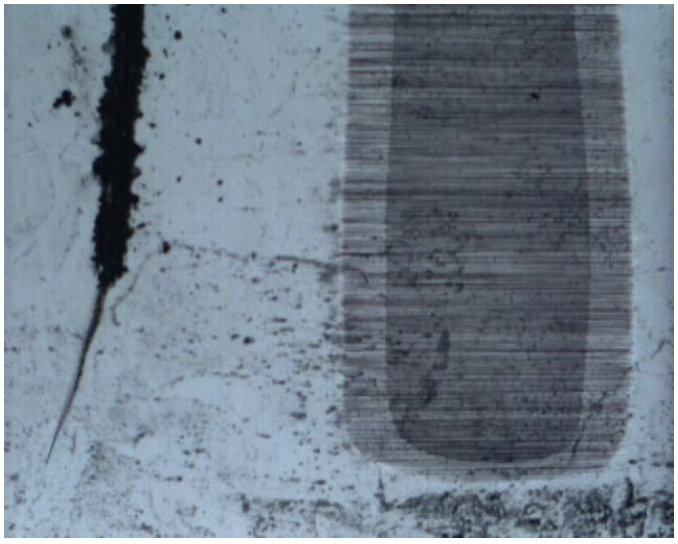


Figure 15. Junction depth (groove and stain) of control wafer 8 or more specifically the junction depth from the first diffusion (n-type).

Junction depth was calculated during step 22 only, as the remainder of the groove and stain tests produced inconclusive results. A successful groove and stain is shown in Figure 15, with a pen mark from a standard BIC pen as a reference. Using the Signatone 1100 groove-and-stain tool, data of z displacement was taken along a standard x-axis. This data was used to form a plot of the profile.

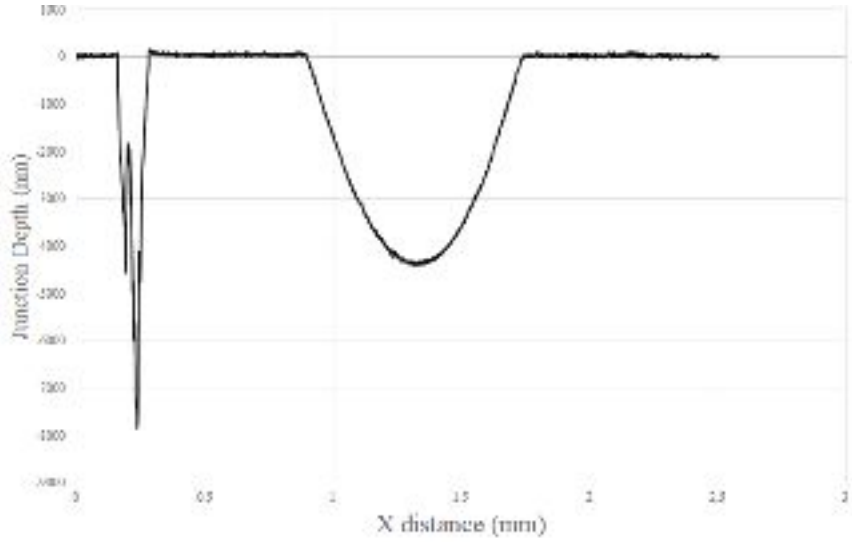



Figure 16. Junction depth (groove and stain) of control wafer 8 or more specifically the junction depth from the first diffusion (n-type)

By comparing the plot and Figure 16, the junction depth was found to be 2.0±0.3 μm.

### iii. Sheet Resistance

The resistivity of all wafers was measured prior to processing to determine a baseline of resistivity for each individual wafer, this data can be seen in Figure 17.

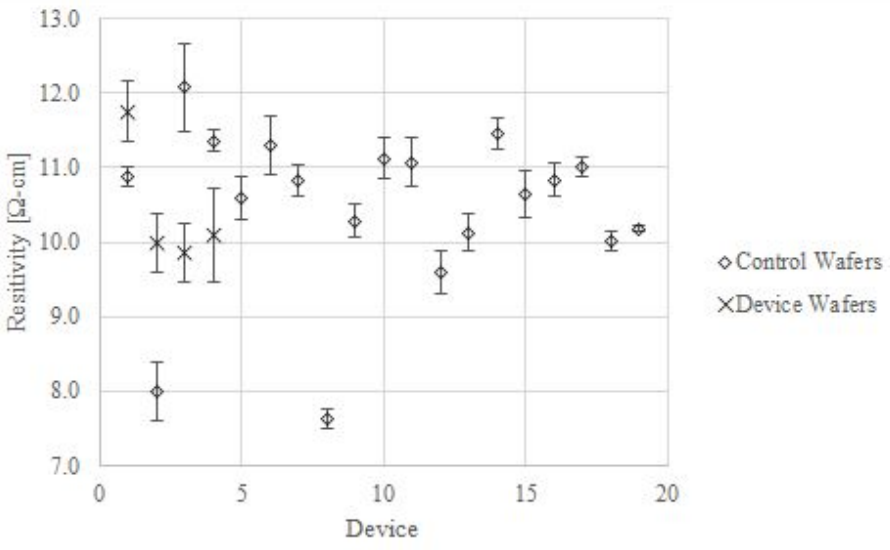



Figure 17. Resistivity across wafer population.

Junction depths were not calculated throughout the processing sequence, this limited our ability to compare resistivity across the sequence. Using a 4-point probe, voltages were collected after each diffusion and etch; these were converted values of resistance which is examined over time in Figure 18.

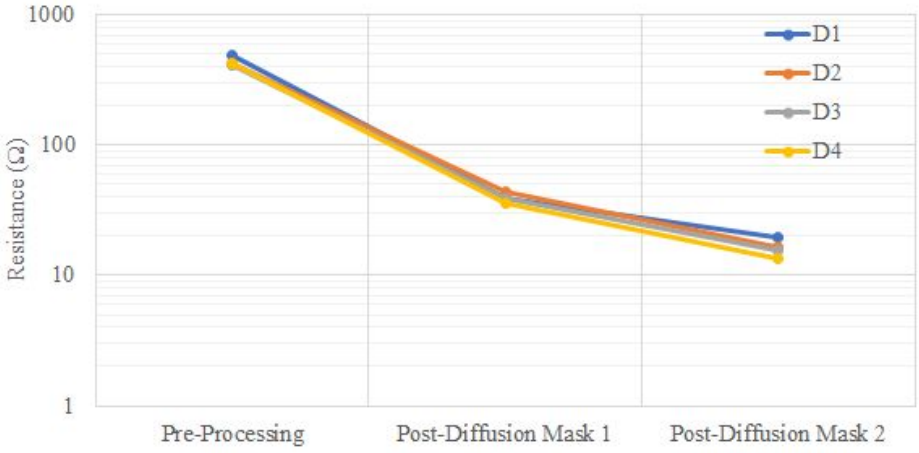



Figure 18. Resistance of device wafers.

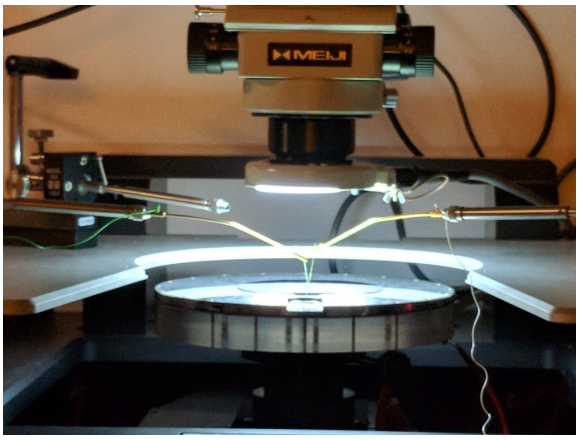
The resistance in the silicon substrate decreased after each diffusion mask iteration, generally decreasing after each processing of the silicon substrate.

## b. Device Testing and Results

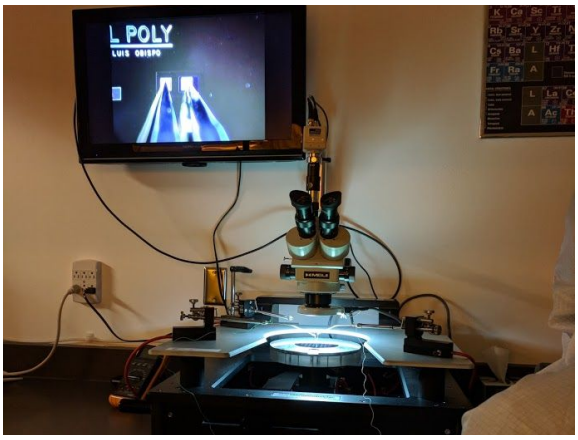
Ultimately, the % yield for diodes was 0%. All the data taken testing diodes suggested resistors were made not didoes. The % yield for resistors was 15%, 96%, and 97% for m, n, and p resistors, respectively. This was based on a rough estimate on the number of resistors that a measurement could be made and those that could not get a measurement.

### i. Test Equipment

In order to test the final devices, resistors and diodes, a prober (probe station), which consists of micromanipulators, a microscope and digital camera, and a special station that has an x and y axis table with a wafer vacuum. The micromanipulators have two needles that can be raised and moved around with fine adjustment knurl screws. These can be connected to a power supply or a multimeter to get measurements.




(a) Close-up




(b) Probe station

Figure 19. Probing station for device testing

## ii. Test Procedure

To test the diodes, a discrete voltage sweep was done across the drain and source of each diode using a power supply, and the current was measured at each voltage difference with an ammeter. This was done for both forward bias and reverse bias. This can be done by simply reversing the polarity of the electrodes. With this, a plot of current vs voltage can be made.

To test the resistors, an ohmeter was placed at the two contacts of one resistor. There were 3 kinds of resistors processed: metal, positive diffused, and negative diffused resistors. For each kind of resistor, there were 6 different sized resistors labelled A-F, going from smallest to largest.

## iii. Diode Results

Based on the current vs voltage curve of the diodes (on C5 and D4), it can be seen that the diodes exhibit the characteristics of a resistor rather than a diode. There is a more linear trend than the characteristic nonlinear curves with a drastic drop at a negative voltage (breakdown) and drastic increase in current in the positive. For a resistor, the I vs V curve's slope is the inverse of the resistance. The grouped data near zero may be just a result of noise since the current measurement could become more sensitive at low voltages.

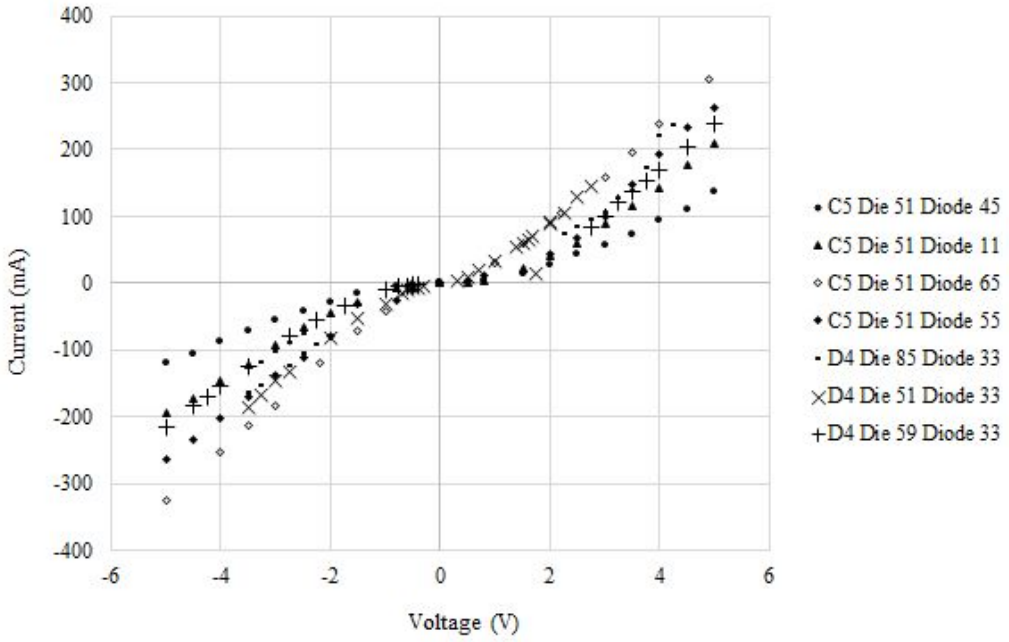
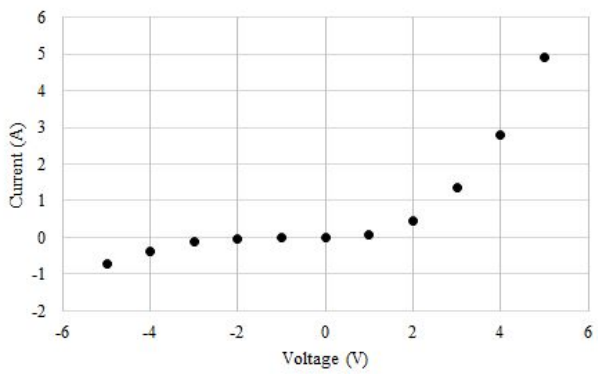
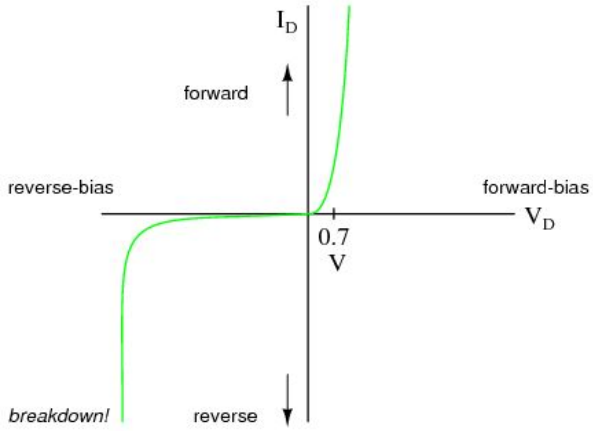



Figure 20. Diode testing I-V curve

Comparing this plot to a working diode, there is a drastic increase in current at about 1 V. However, this plot obtained from a supposed working diode was cut off and the breakdown is not shown. The difference becomes much more apparent when the data is compared to the theoretical curve for a diode.




(a) No dopant control wafers




(b) Doped wafers

Figure 21. Working diode and theoretical diode curve

Based on the comparison, the diodes were not functioning as diodes but as resistors.

## iv. Resistor Results

The values of the resistance for each type of resistor and size is shown below. Overall, n-type resistors had the highest resistance, followed by p-type, and lastly metal. This is consistent throughout all three resistor sizes. Also, as expected the nominal values show an increase in resistance with the bigger resistors. The n-type resistors did break this trend between A and B size resistors. However, it is important to note that the uncertainties of for the two averages do agree/overlap.

Table 21. Resistances (Ω) of the mean of metal, n-type, and p-type resistors across devices

| Size | Metal (Ω) | p-Type (Ω) | n-Type (Ω) |
|---|---|---|---|
| A | 2.21E+01 ± 9.9E+00 | 2.48E+03 ± 6.5E+02 | 1.34E+06 ± 5.9E+05 |
| B | 2.66E+01 ± 0.53E+01 | 3.36E+03 ± 1.39E+03 | 1.14E+06 ± 6.6E+05 |
| F | 7.35E+01 ± 2.14E+01 | 1.08E+05 ± 8.2E+04 | 1.02E+07 ± 1.50E+07 |

The large uncertainty may be a result of several factors. These values came from different dies. Different areas of the wafer may have had different amounts of dopant and/or oxides. Some of the uncertainties are larger than the nominal value.

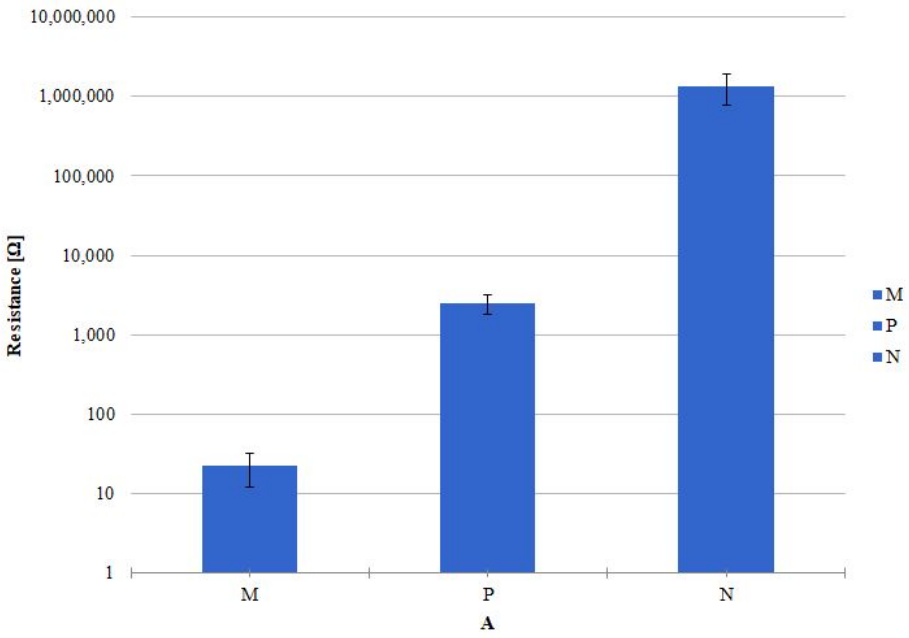



Figure 22. Resistor type A resistance values

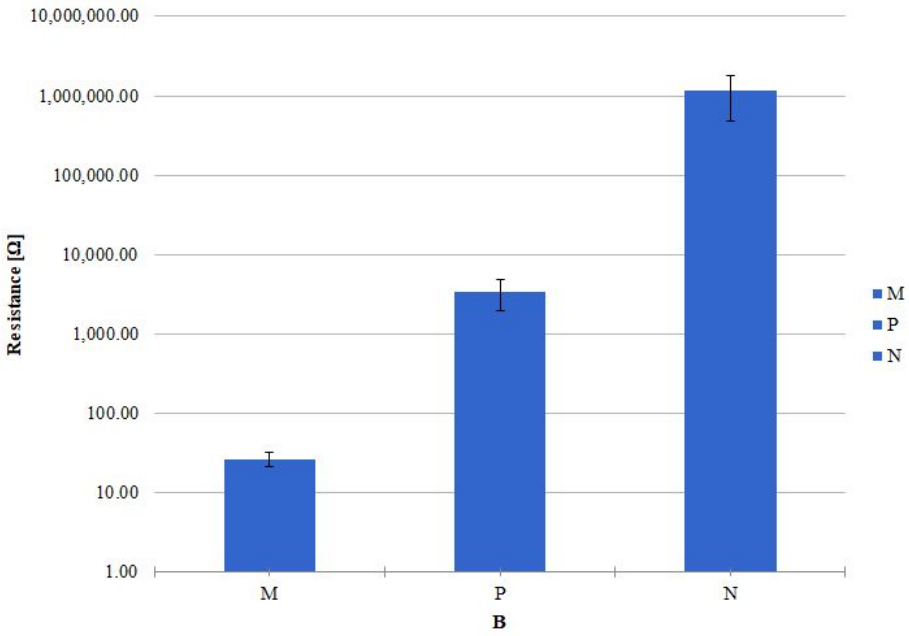



Figure 23. Resistor type B resistance values

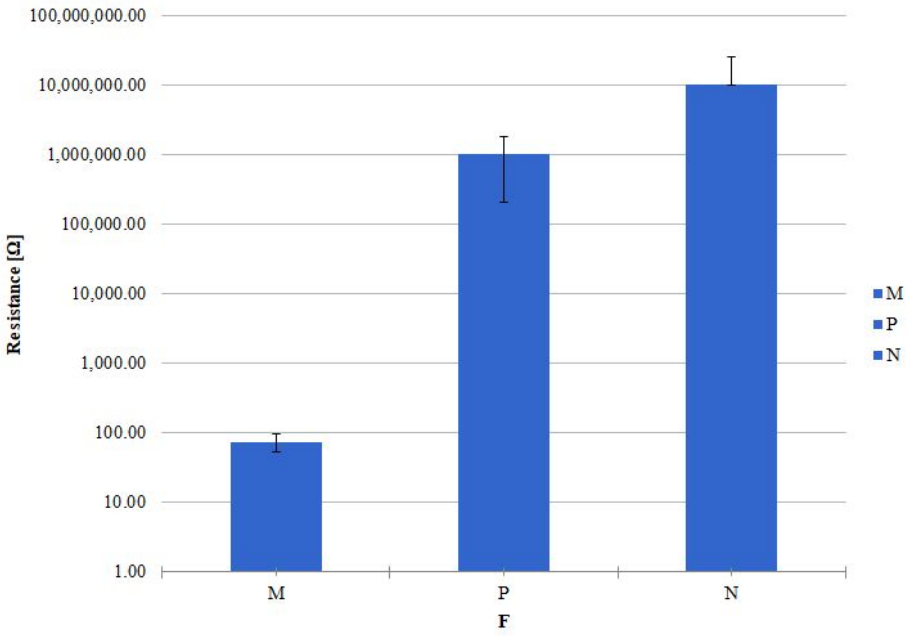



Figure 24. Resistor type F resistance values.

The resistance uncertainty on Figure 24 for n-type is so large that the plot does not show it due to a zero error on the log-scale.

## c. Possible Errors

There are many possible factors that could help led to the unsuccessful fabrication of diodes. Some major factors that may have led to the failed diodes are listed below.

1. Expired dopants: the p-type dopant used for the second diffusion was expired
    a. Proof:
        i. There were no successful groove and stains with the second diffusion with the p-type dopant.
    b. Counterproof:
        i. There is a measured difference between resistivity after the diffusion with the dopant.
2. Over oxidation: the water heater for a different oven had been left on
    a. Proof:
        i. It was noted that the water heater for a lower oven was left on, causing a longer oxidation time than what was calculated/intended for the second diffusion mask. Furthermore, it was noted that the device oxide thickness was much larger than expected for the second mask.
    b. Counterproof:
        i. Even with the thick oxide layer, the wafers were able to get doped based on visual inspection and resistivity values measured.
3. Insufficient field oxide:
    a. Proof:
        i. It was noted that the $O_2$ had not been turned on during the field oxide growth until the last 35 minutes of the cycle.
    b. Counterproof:

i. Based on oxide thickness measurements, it can be seen that the even though the oxidation time was shortened, a sufficient layer of oxide was grown.

These are all speculations and further testing could definitively show if these reasons could cause the diodes to act as a resistor.

# Conclusions

Processing of diodes was not successful, but thin-film and diffused resistors were created. The diodes could be a result of several factors such as expired dopant which could of led to insufficient diffusion, over oxidation which could have grown through the first diffusion, and insufficient field oxide which could have led to a short in the aluminum. Though diodes were not successfully fabricated, this processing brought in a greater insight on microfabrication. From wafer selection to device testing, it showed the meticulous, care, planning, and organization required to manufacture even simple components such as resistors and diodes.

The processing gave an introduction to many of the fundamental unit processes in microfabrication: cleaning, oxidation, spin coating, exposing resist, developing resist, etching, stripping resist, diffusion, and sputtering. These can be extended to create more complex components. There are similarities between the all the processes for used in microfabrication. Though the medium and method may differ, the overall process consists of adding and removing material, and patterning is used to select how or what is added and removed.

Metrology encompasses much of the microfabrication. This is a direct result of the small nature of the parts being manufactured. Unlike, machining where a visual inspection or tools such as calipers and gage pins can measure the size of features, microfabrication requires much more complicated and precise tools to measure features. Control wafers serve a vital role in maintaining a record for quality that can be used to determine the issues with processing.

If more studies could be done, an in depth look at each of the control wafers could provide more insight on the possible error(s) that led to the failed diodes. It would also be interesting to test each of the possible errors to see if they do in fact have an effect.

On a more personal note, if we could do this processing again with the knowledge we have now at the end, we would have completely approached the lab differently. It is partially our fault for not learning ahead, but many of the aspects of this lab were only truly realized just a bit too late. There are no problems with that because being forced to learn and making a blind attempt first did solidify the knowledge.

The need for communication cannot be overstated. So many of the steps in the sequence are interconnected and many steps work in. Any miscommunication or lack of communication had a massive impact.

This processing gave a glimpse of how the smallest things can make a huge difference.

# References

[1] Campbell, Stephen A. *Fabrication Engineering at the Micro- and Nanoscale*. 4th ed., Oxford University Press, 2013.

[2] Savage, Richard. “Lecture 1: Fabricating Devices at the Micro/Nano Scale.” 2018. *Microsoft PowerPoint* file.

[3] “Introduction to Diodes and Rectifiers.” *All About Circuits*, www.allaboutcircuits.com/textbook/semiconductors/chpt-3/introduction-to-diodes-and-rectifiers/.

[4] “Resistor Fabrication on Semiconductor Wafers - Diffused, Ion-Implanted, Thin-Film, Polysilicon”. *EESemi*, 2005, www.eesemi.com/resistor-fab.htm.

[5] Lewis, Kim. “Uses of Resistors.” *Sciencing*, 13 Mar. 2018, sciencing.com/uses-resistors-5432023.html.

[6] Savage, Richard. "Lecture 7: Lithography." 2018. *Microsoft PowerPoint* file.

[7] Savage, Richard. “Lecture 1B: Microfabrication Processes & Materials.” 2018. *Microsoft PowerPoint* file.

[8] Del Aguila, Jeremy. “Diode Fab.” 2018. *PNG* file.

[9] *High Temperature Furnace SOP*. 2013, *High Temperature Furnace SOP*.

[10] Jaeger, Richard C. *Introduction to Microelectronic Fabrication*. 2nd ed., Prentice Hall, 2002.

[11] Savage, Richard. “Lecture: Photolithography - Resists.” 2018. *Microsoft PowerPoint* file.

[12] Williams, K.r., and R.s. Muller. “Etch Rates for Micromachining Processing.” Journal of Microelectromechanical Systems, vol. 5, no. 4, 1996, pp. 256–269., doi:10.1109/84.546406.

[13] Savage, Richard. "Lecture 3: Diffusion." 2018. *Microsoft PowerPoint* file.

# Appendix A: Equipment

| Step | Equipment | Extra Materials/Chemicals |
|---|---|---|
| Cleaning | SEMITOOL PSC-101 SRD | Teflon cassette and handle<br>DI water<br>Piranha*<br>BOE (Buffered oxide etch)<br>$N_2$ |
| Oxidation | STT-1200C-6-12 | $N_2$<br>$O_2$<br>$H_2O$<br>Quartz boat |
| Spin coating | Laurell WS-400BZ-6NPP/LTE | Shipley S1813<br>Dopants<br>Eppendorf Pipette<br>HMDS Primer 80/20<br>Luer tip dispensing syringe |
| Expose | GAMM (Quintel) Aligner | N/A |
| Develop | N/A | Teflon cassette<br>Microposit CD-26 (2.5% TMAH)<br>Glass beaker<br>DI Water |
| Etch | N/A | Teflon cassette<br>Glass beakers<br>Hot plate<br>BOE (Buffered oxide etch)<br>DI Water |
| Strip | N/A | Teflon cassette<br>Microposit Remover 1165 |
| Diffusion | STT-1200C-6-12 | $N_2$<br>$O_2$<br>Quartz boat |
| Sputtering | Rohwedder sputtering system | Aluminum target; Argon |
| Sheet resistance | S-301 4-pt Probe | N/A |
| Film thickness | Filmetrics F20 | N/A |
| Junction depth | Signatone 1100 | Stain |
| Prober | Meiji microscope | Multimeter, micromanipulator |
| Microscope | - | - |

* Sulfuric acid ($H_2SO_4$) and hydrogen peroxide ($H_2O_2$)

## Appendix A: Equipment (Cont'd)


Cleaning SRD


Cleaning, strip, and etching station

## Appendix A: Equipment (Cont'd)


High temp furnace (oxidation and diffusion)


Spin coating station

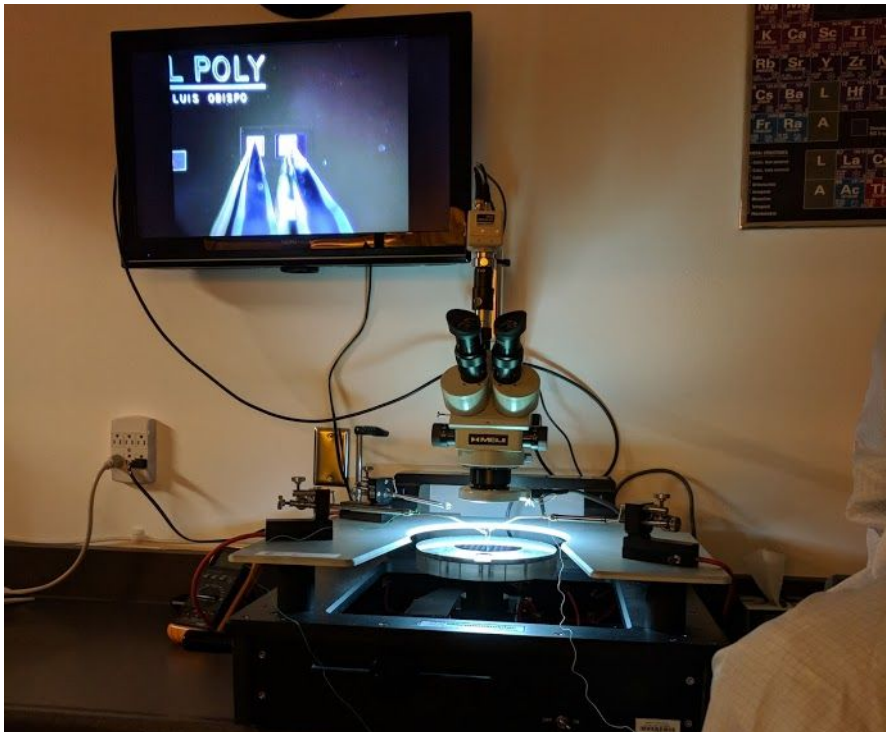
## Appendix A: Equipment (Cont'd)


GAMM aligner

Developer station

## Appendix A: Equipment (Cont'd)

Filmetrics F20




Prober station

## Appendix A: Equipment (Cont'd)


Microscope (visual inspection) station

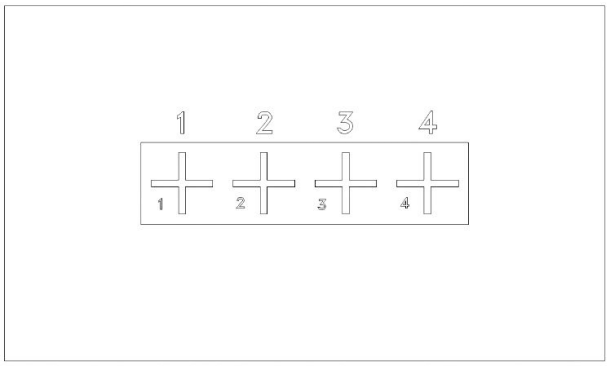
NOTE: The sputtering, 4-pt probe, and groove and stain equipment are not shown. Many of the extra materials required are also not shown.

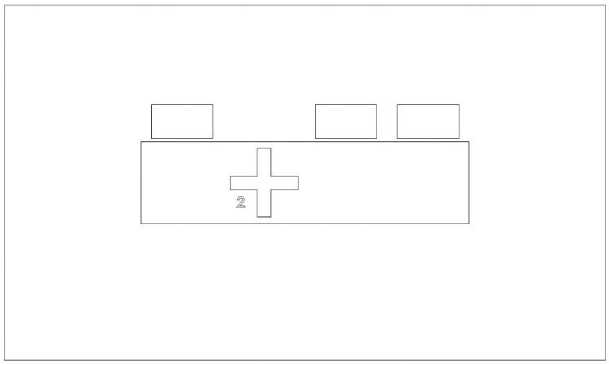
# Appendix B: Full Process Flow

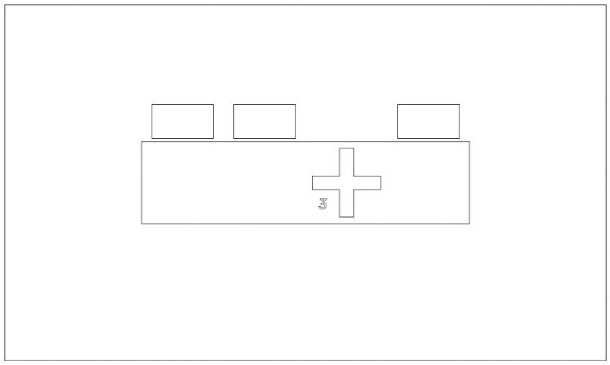
| Step | Process | Device ( D ) | | | | Control ( C ) | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | D1 | D2 | D3 | D4 | C1 | C2 | C3 | C4 | C5 | C6 | C7 | C8 | C9 | C10 | C11 | C12 | C13 | C14 | C15 | C16 | C17 | C18 | C19 |
| 1 | select wafers | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| 2 | scribe wafers | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| 3 | wafer thickness measurements | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| 4 | clean wafers (Piranha & BOE) | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| 5 | measure sheet resistance | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| 6 | grow diffusion mask 1 | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| 7 | measure diffusion mask oxide thickness | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| 8 | clean wafers (Piranha) | • | • | • | • | • | • | • | • | • | | | | | | | | | | | | | | |
| 9 | spin coat photoresist (S 1813) | • | • | • | • | • | • | • | • | • | | | | | | | | | | | | | | |
| 10 | expose diffusion mask 1: MASK #1 | • | • | • | • | | • | • | • | • | | | | | | | | | | | | | | |
| 11 | develop wafers (CD-26) | • | • | • | • | | • | • | • | • | | | | | | | | | | | | | | |
| 12 | measure oxide etch rate (BOE) | | | | | | | | | | ◙ | • | | | | | | | | | | | | |
| 13 | etch diffusion mask (BOE) | • | • | • | • | • | • | • | • | • | | | • | • | • | • | • | • | • | • | • | • | • | • |
| 14 | remove photoresist (1165) | • | • | • | • | • | • | • | • | • | | | | | | | | | | | | | | |
| 15 | clean wafers (Piranha) | • | • | • | • | • | ◙ | • | • | • | | • | • | • | | | • | • | | • | • | • | • | • |
| 16 | spin on dopant (p-type: boron B155) | • | • | • | • | • | | • | • | • | | • | • | • | | | | | | • | • | | | |
| 17 | diffusion 1: p-type pre-dep | • | • | • | • | • | | • | • | • | | • | • | • | | | • | • | | • | • | • | • | • |
| 18 | measure diffusion mask oxide thickness | • | • | • | • | • | | • | • | • | | • | • | • | | | • | • | | • | • | • | • | • |
| 19 | etch diffusion mask (BOE) | • | • | • | • | • | | • | • | • | | • | • | • | | | • | • | | • | • | • | • | • |
| 20 | measure sheet resistance (p pd) | • | • | • | • | • | | • | • | • | | | • | • | | | | | | • | • | | | |
| 21 | measure diffusion mask effectiveness (p pd) | | | | | | | | | | | ◙ | | | | | | | | | | | | |
| 22 | measure junction depth (p pd) | | | | | | | | | | | | ◙ | | | | | | | | | | | |
| 23 | clean wafers (Piranha & BOE) | • | • | • | • | • | | • | • | • | | | | • | • | | • | • | | • | • | • | • | • |
| 24 | grow diffusion mask 2 & p di1 | • | • | • | • | • | | • | • | • | | | | • | • | | • | • | | • | • | • | • | • |
| 25 | measure diffusion mask oxide thickness | • | • | • | • | | | • | • | • | | | | • | • | | | | | | | • | • | • |
| 26 | measure sheet resistance (p pd+di1) | | | | | | | | | | | | | • | | | | | | | • | | | |
| 27 | measure junction depth (p pd+di1) | | | | | | | | | | | | | ◙ | | | | | | | | | | |
| 28 | clean wafers (Piranha) | • | • | • | • | • | | • | • | • | | | | | | | | | | • | • | | | |
| 29 | spin coat photoresist (S1813) | • | • | • | • | • | | • | • | • | | | | | | | | | | | | | | |
| 30 | expose diffusion mask 2: MASK #2 | • | • | • | • | | | • | • | • | | | | | | | | | | | | | | |
| 31 | develop wafers (CD-26) | • | • | • | • | | | • | • | • | | | | | | | | | | | | | | |
| 32 | measure oxide etch rate (BOE) | | | | | | | | | | | | | | • | | | | | | | | | |
| 33 | etch diffusion mask (BOE) | • | • | • | • | • | | • | • | • | | | | | | | • | • | | • | • | | | |
| 34 | remove photoresist (1165) | • | • | • | • | | | • | • | • | | | | | | | | | | | | | | |
| 35 | clean wafers (Piranha) | • | • | • | • | • | | ◙ | • | • | | | | | • | • | • | • | | • | • | • | • | • |
| 36 | spin on dopant (n-type: phosphorus P507) | • | • | • | • | • | | | • | • | | | | | • | • | | • | | | • | | | |
| 37 | diffusion 2: n-type pre-dep + p di 2 | • | • | • | • | • | | | • | • | | | | | • | • | • | • | | • | • | • | • | • |
| 38 | measure diffusion mask oxide thickness | • | • | • | • | • | | | • | • | | | | | • | • | | | | • | • | • | • | • |
| 39 | etch diffusion mask (BOE) | • | • | • | • | • | | | • | • | | | | | • | • | | | | • | • | • | • | • |
| 40 | measure sheet resistance (n pd) | • | • | • | • | | | | • | • | | | | | | • | | | | | | | | |
| 41 | measure diffusion mask effectiveness (n pd) | | | | | | | | | | | | | | ◙ | | | | | | | | | |
| 42 | measure junction depth (n pd) | | | | | | | | | | | | | | | ◙ | | | | | | | | |
| 43 | measure sheet resistance (p pd+di1+di2) | | | | | | | | | | | | | | | | | | | • | | | | |
| 44 | measure junction depth (p pd+di1+di2) | | | | | | | | | | | | | | | | ◙ | | | | | | | |
| 45 | measure junction depth (n pd + p pd+di1+di2) | | | | | | | | | | | | | | | | | ◙ | | | | | | |
| 46 | clean wafers (Piranha & BOE) | • | • | • | • | • | | | • | • | | | | | | | | | • | • | • | • | • | • |
| 47 | grow field oxide & n/p drive-in | • | • | • | • | • | | | • | • | | | | | | | | | • | • | • | • | • | • |
| 48 | measure diffusion mask oxide thickness | • | • | • | • | • | | | • | • | | | | | | | | | • | • | • | • | • | • |
| 49 | measure sheet resistance (n pd + di1) | | | | | | | | | | | | | | | | | | • | | | | | |
| 50 | meausure junction depth (n pd + di1) | | | | | | | | | | | | | | | | | | ◙ | | | | | |
| 51 | measure sheet resistance (p pd+di1+di2+di3) | | | | | | | | | | | | | | | | | | | • | | | | |
| 52 | measure junction depth (p pd+di1+di2+di3) | | | | | | | | | | | | | | | | | | | ◙ | | | | |
| 53 | measure junction depth (n pd + p pd+di1+di2+di3) | | | | | | | | | | | | | | | | | | | | ◙ | | | |
| 54 | clean wafers (Piranha & BOE) | • | • | • | • | • | | | • | • | | | | | | | | | | | | | | |
| 55 | spin coat photoresist (S1813) | • | • | • | • | • | | | • | • | | | | | | | | | | | | | | |
| 56 | expose field oxide: MASK #3 | • | • | • | • | | | | • | • | | | | | | | | | | | | | | |
| 57 | develop wafers (CD-26) | • | • | • | • | | | | • | • | | | | | | | | | | | | | | |
| 58 | etch diffusion mask (BOE) | • | • | • | • | • | | | • | • | | | | | | | | | | | | | | |
| 59 | remove photoresist (1165) | • | • | • | • | • | | | • | • | | | | | | | | | | | | | | |
| 60 | clean wafers (Piranha) | • | • | • | • | • | | | ◙ | • | | | | | | | | | | | | • | • | • |
| 61 | sputter aluminum film (Rohwedder system) | • | • | • | • | • | | | | • | | | | | | | | | | | | • | • | • |
| 62 | measure aluminum film thickness | • | • | • | • | • | | | | • | | | | | | | | | | | | ◙ | • | • |
| 63 | measure aluminum film sheet resistance | • | • | • | • | • | | | | • | | | | | | | | | | | | | ◙ | • |
| 64 | spin coat photoresist (S1813) | • | • | • | • | • | | | | • | | | | | | | | | | | | | | |
| 65 | expose metal removal: MASK #4 | • | • | • | • | | | | | • | | | | | | | | | | | | | | |
| 66 | develop wafers (CD-26) | • | • | • | • | | | | | • | | | | | | | | | | | | | | |
| 67 | aluminum etch test (measure rate) | • | • | • | • | | | | | • | | | | | | | | | | | | | | ◙ |
| 68 | etch aluminum film to form contacts | • | • | • | • | | | | | • | | | | | | | | | | | | | | |
| 69 | remove photoresist (1165) | • | • | • | • | ◙ | | | | ◙ | | | | | | | | | | | | | | |
| 70 | measure test chips (diodes) | ◙ | ◙ | ◙ | ◙ | | | | | | | | | | | | | | | | | | | |
| 71 | measure test chips (diffused resistors) | ◙ | ◙ | ◙ | ◙ | | | | | | | | | | | | | | | | | | | |
| 72 | measure test chips (thin-film resistors) | ◙ | ◙ | ◙ | ◙ | | | | | | | | | | | | | | | | | | | |

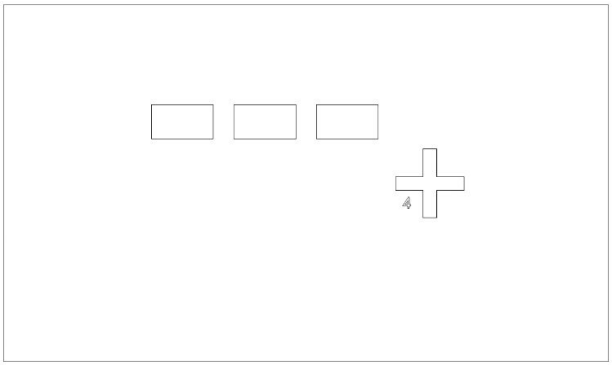
# Appendix C: Masks and Alignment Marks

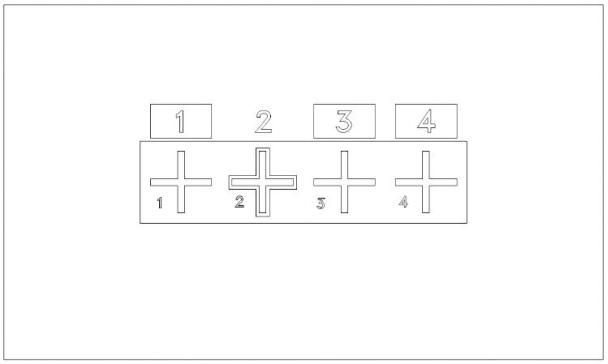
## Alignment Marks

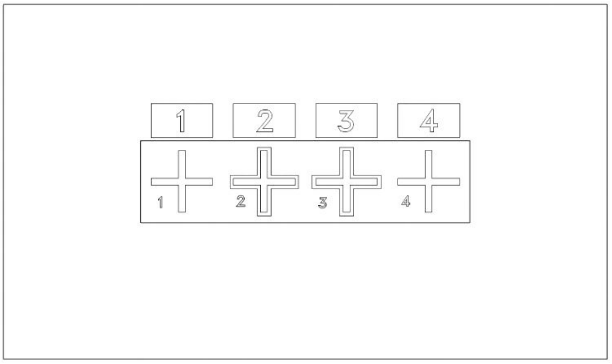


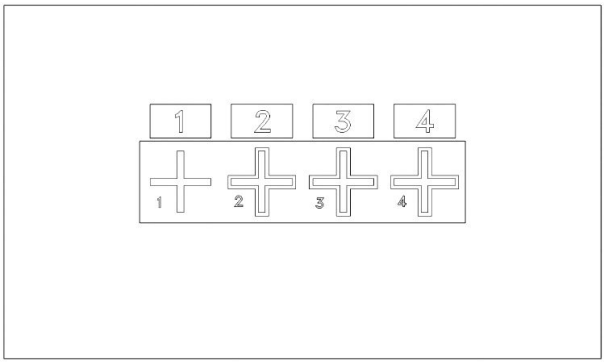



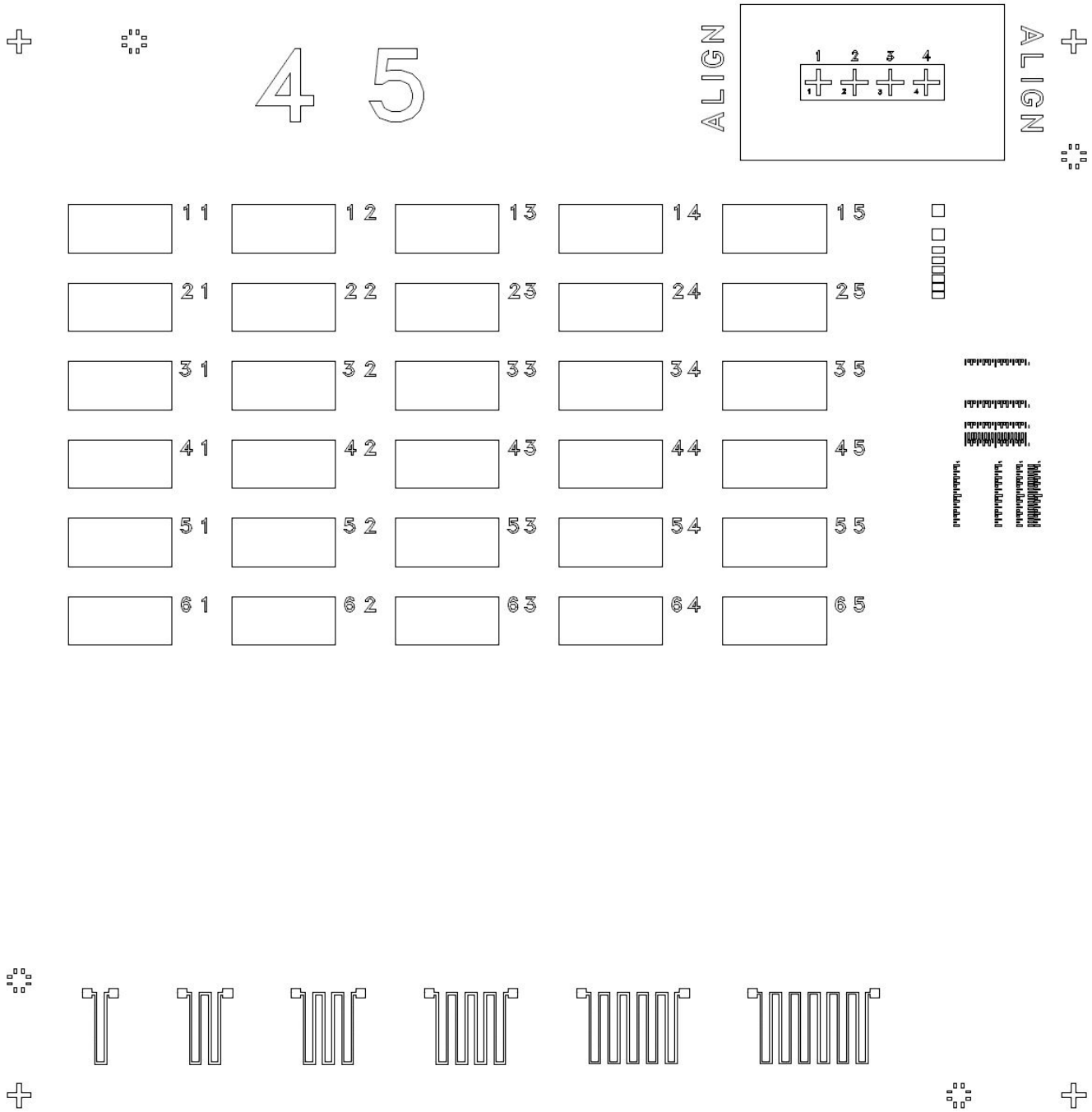



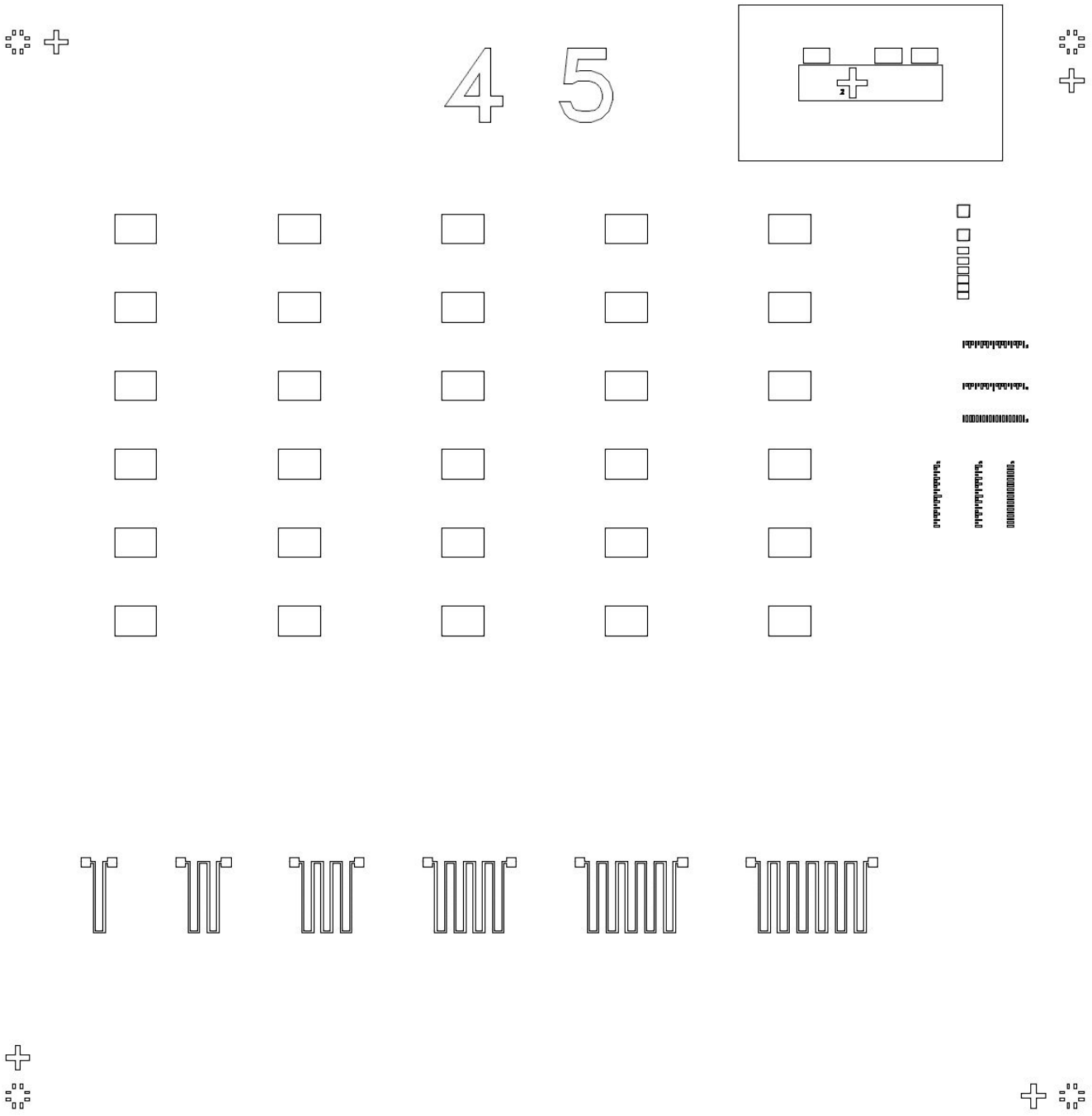



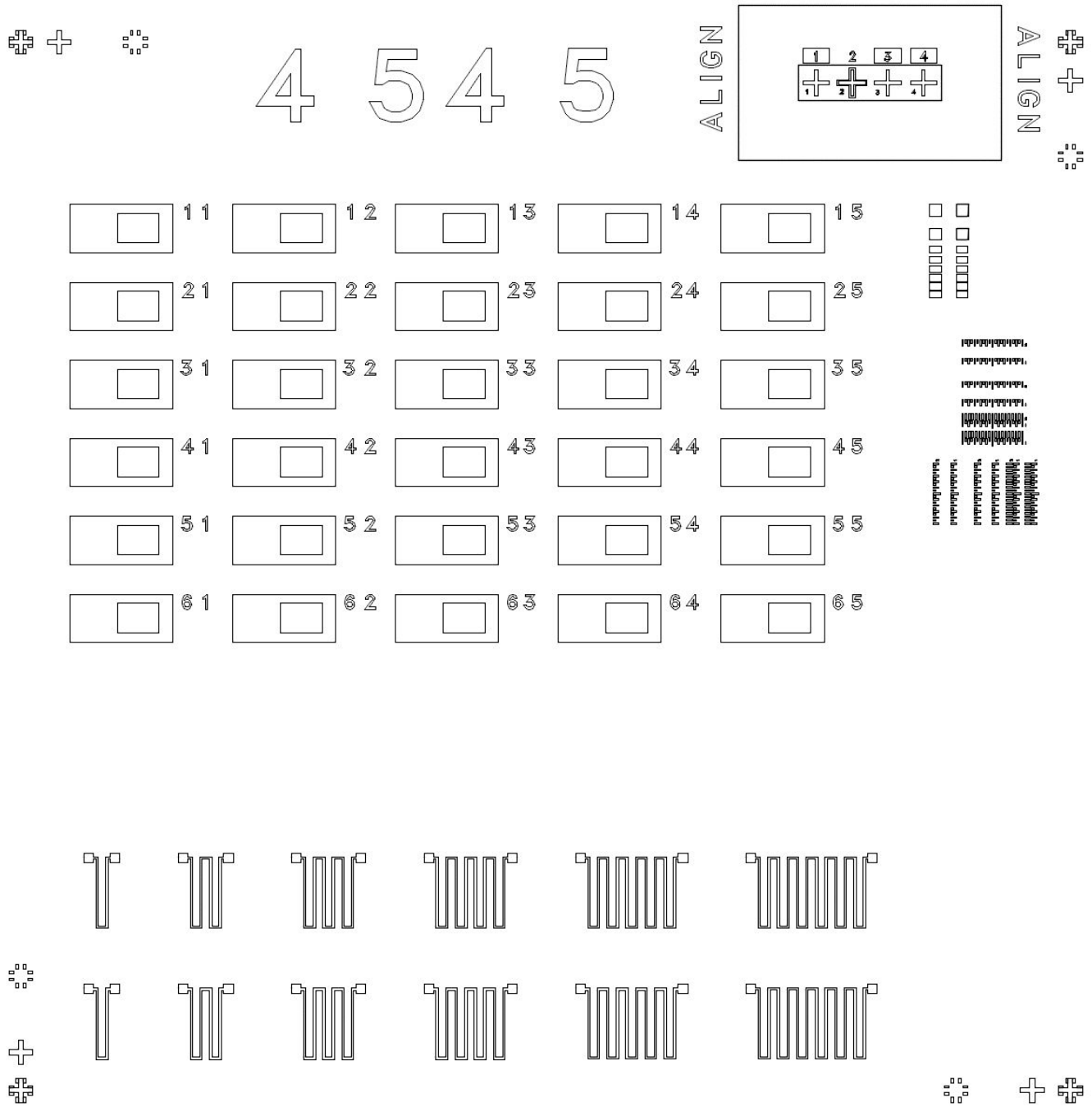
## Appendix C: Masks and Alignment Marks (Cont'd)
## Mask #1



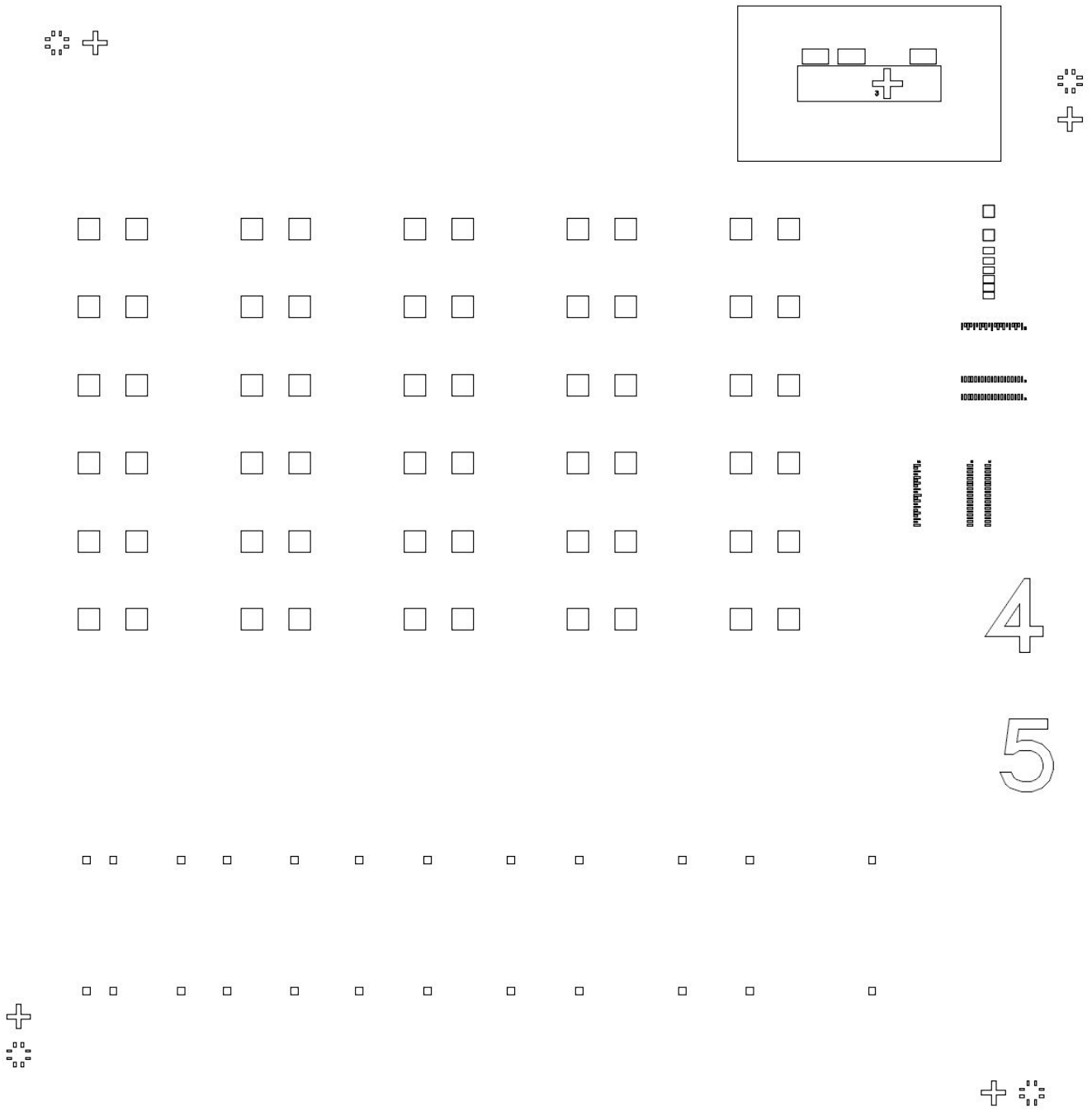
## Appendix C: Masks and Alignment Marks (Cont'd)
## Mask #2



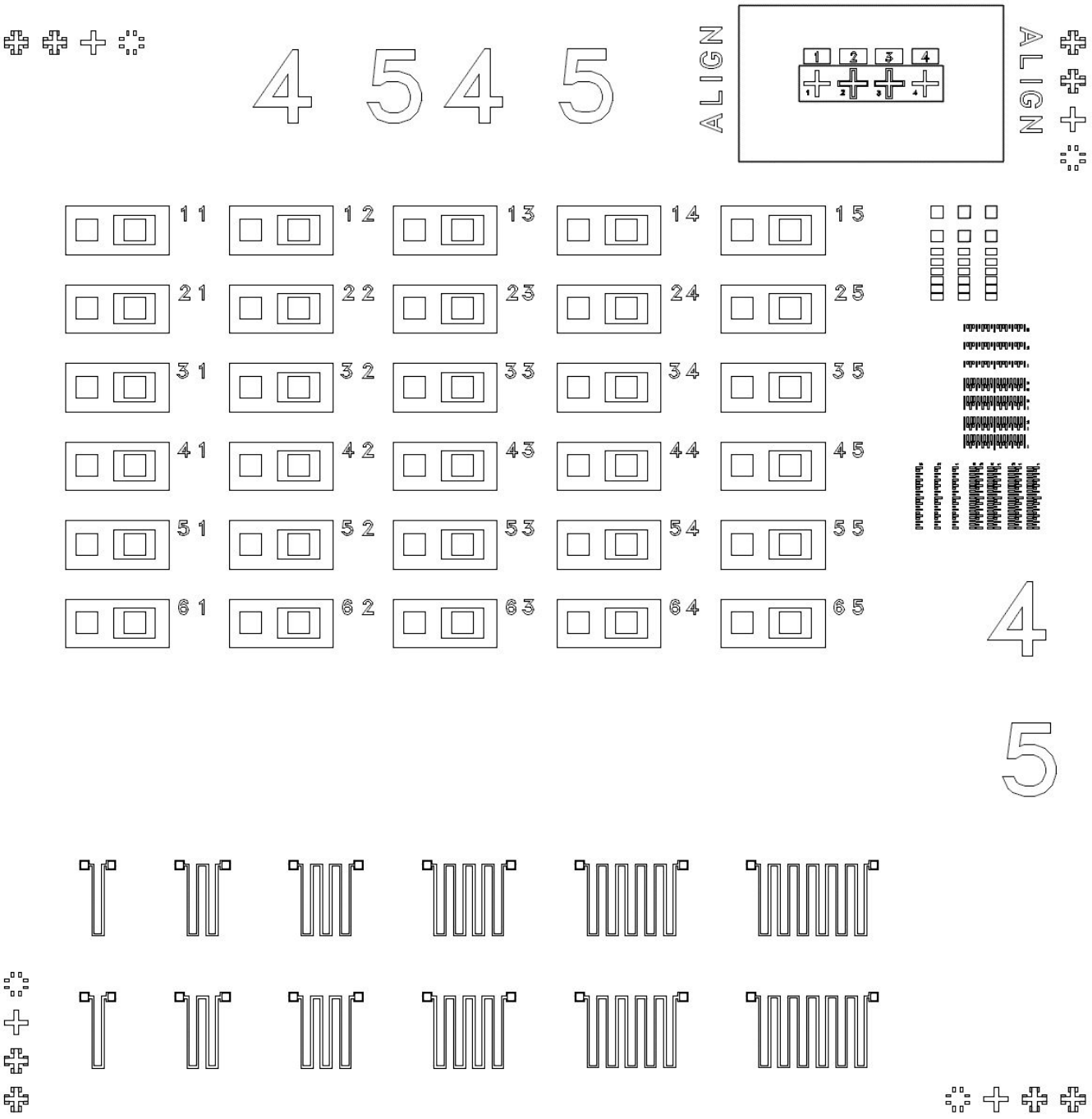
## Appendix C: Masks and Alignment Marks (Cont'd)
## Mask #1 and 2



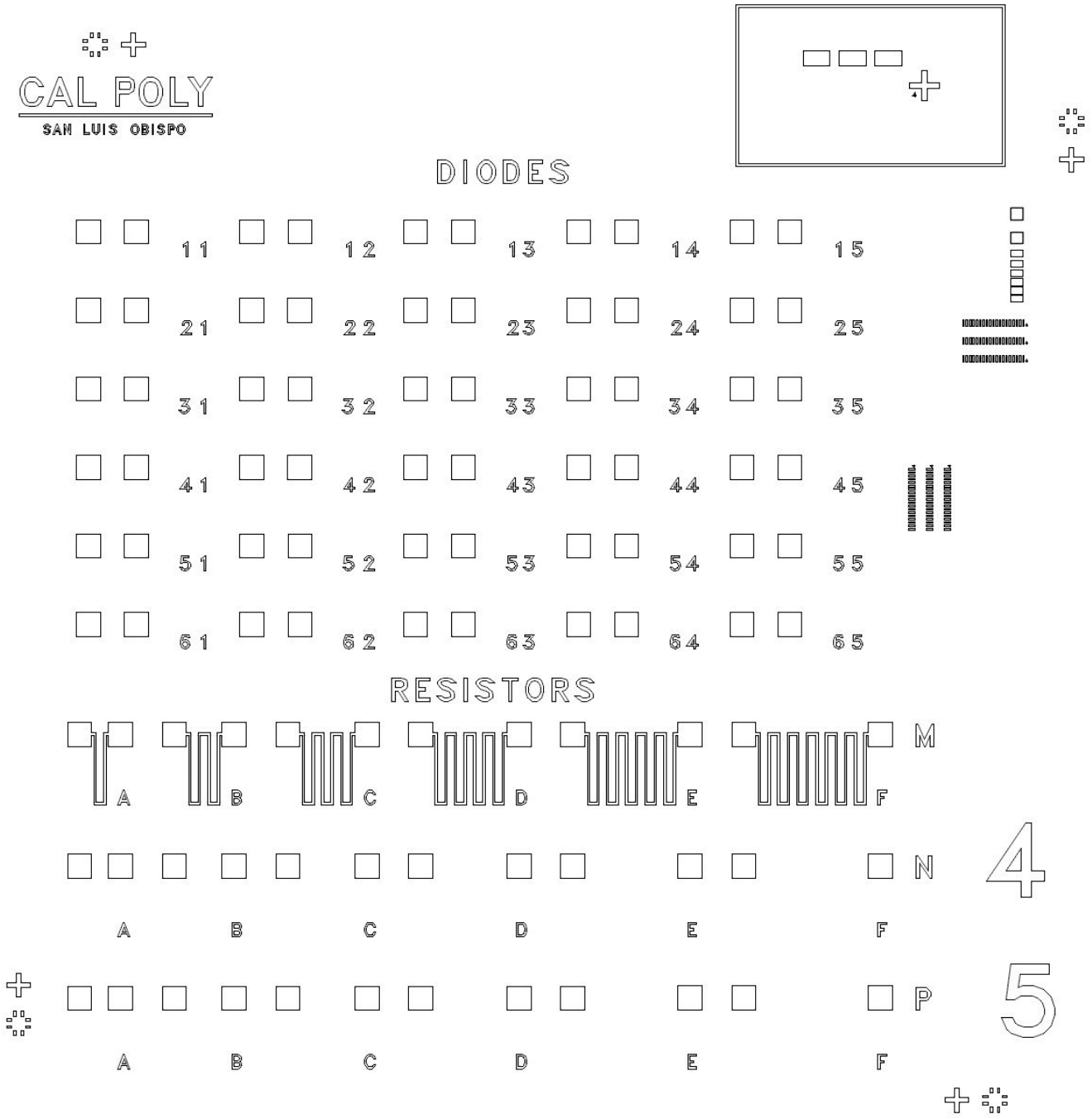
## Appendix C: Masks and Alignment Marks (Cont'd)
## Mask #3



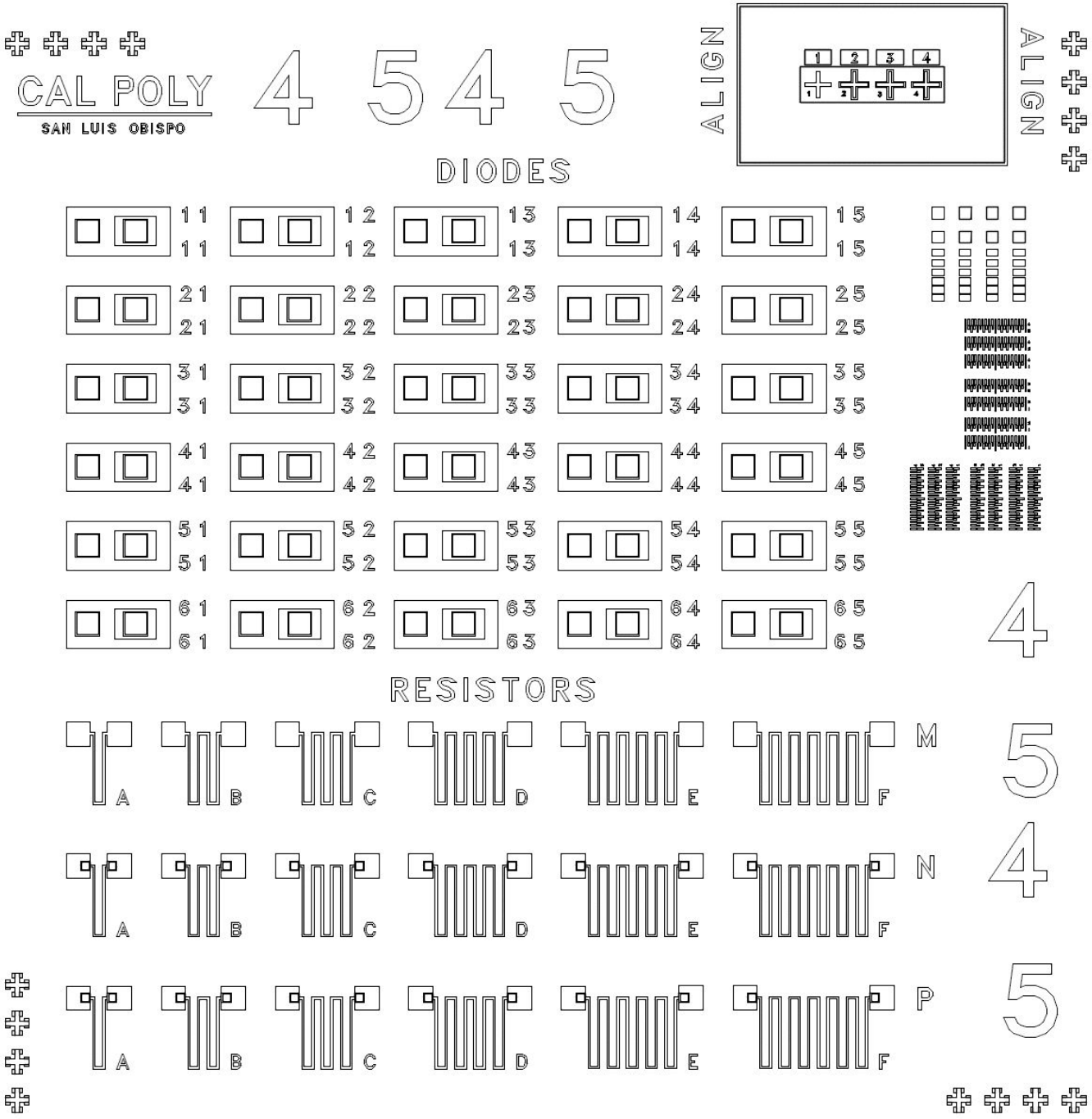
## Appendix C: Masks and Alignment Marks (Cont'd)
## Mask #1, 2, and 3



## Appendix C: Masks and Alignment Marks (Cont'd)
## Mask 4



## Appendix C: Masks and Alignment Marks (Cont'd)
## All Masks



# Appendix D: Control Wafers

| Wafer | General Purpose | Detailed Purpose | Metrology |
|---|---|---|---|
| C1 | Exposure matrix | Exposure matrix, visual inspection wafer | Microscope |
| C2 | Diffusion mask | Diffusion (diff) mask 1; inspect diff mask 1 after etch | Profilometer |
| C3 | | Diff mask 1 and 2 thickness; inspect diff mask 2 after etch | Profilometer |
| C4 | | Diff mask 1, 2, and 3 thickness and inspect diff mask 3 after etch | Profilometer |
| C5 | Aluminum etch | Aluminum etch depth; contact area inspection | Profilometer |
| C6 | Etch rate | Diff mask 1; oxide etch rate | SR |
| C7 | Etch rate, resistance | Oxide etch rate; diff 1 mask resistance | SR; 4-point probe |
| C8 | Resistance | Resistance of diff 1; positive (pos) predoposition (predep) junction depth | 4-point probe; G+S |
| C9 | | Resistance of diff 1; positive predep and drive-in 1 junction depth | 2x 4-point probe; G+S |
| C10 | Etch rate, resistance | Pos drive in etch rate, negative (neg) predep mask resistance | SR; 4-point probe |
| C11 | Junction depth | Neg predep junction depth | G+S |
| C12 | | Junction depth (pos predep for drive-in 1 and 2) | G+S |
| C13 | | Junction depth (pos and neg predep for drive-in 1 and 2) | G+S |
| C14 | Field oxide | Field oxide resistance; field oxide junction depth | 4-point probe; G+S |
| C15 | Resistance and junction depth | Resistance of diff mask 1 and 2; pos predep and di 1, 2, and 3; junction depth | 3x 4-point probe; G+S |
| C16 | | Resistance of diff 1; junction depth of neg predep, pos predep, di 1, 2, and 3 | 2x 4-point probe; G+S |
| C17 | Diffusion mask and aluminum film | Diffusion mask thicknesses; aluminum film thickness; sputtering performance | 4x Profilometer |
| C18 | | Diffusion mask thicknesses; aluminum sheet resistance from sputtering | 3x Profilometer; 4-point probe |
| C19 | | Diffusion mask thicknesses; aluminum etch rate test for aluminum | 4x Profilometer |

SR: sheet resistance
G+S: groove and stain

Many wafers have multiple purposes to be more economical with the wafers. Some metrology steps are destructive, such as groove and stain, but until a destructive test needs to be completed on a wafer, that wafer can be utilized to get other measurements.

# Appendix E: Processing Data and Calculations

| Oxide Thickness [nm] STEP 7 | | | | | | |
|---|---|---|---|---|---|---|
| Wafer | Average | Max | Min | Range (Max-Min) | Std. Dev | Uncertainty |
| D1 | 504.4 | 512.5 | 501 | 11.5 | 4.7 | 5.8 |
| D2 | 507.5 | 512.2 | 504.5 | 7.7 | 3 | 3.8 |
| D3 | 514.2 | 516.2 | 512.5 | 3.7 | 1.8 | 2.2 |
| D4 | 520.9 | 524.8 | 517.9 | 6.9 | 3.5 | 4.3 |
| C1 | 327.8 | 337.3 | 313.7 | 23.6 | 9.7 | 12.1 |
| C2 | 359.4 | 377.2 | 342.3 | 34.9 | 14 | 17.4 |
| C3 | 393.9 | 400.5 | 387.1 | 13.4 | 5.4 | 6.7 |
| C4 | 422.1 | 430.9 | 412.7 | 18.1 | 8.2 | 10.2 |
| C5 | 442 | 449.9 | 435.1 | 14.8 | 7.1 | 8.9 |
| C6 | 460.1 | 468.8 | 454.1 | 14.7 | 6.3 | 7.8 |
| C7 | 469.8 | 473.9 | 464.3 | 9.6 | 3.8 | 4.7 |
| C8 | 477.8 | 480.2 | 473.9 | 6.3 | 2.5 | 3 |
| C9 | 489.2 | 494.2 | 485.8 | 8.4 | 3.7 | 4.6 |
| C10 | 505.8 | 509.3 | 503.7 | 5.7 | 2.7 | 3.3 |
| C11 | 529.3 | 532 | 527.2 | 4.8 | 2.4 | 2.9 |
| C12 | 530.6 | 532.9 | 528.4 | 4.5 | 2.2 | 2.7 |
| C13 | 530.6 | 533.4 | 528.9 | 4.5 | 2 | 2.5 |
| C14 | 538.5 | 540.4 | 536 | 4.3 | 1.7 | 2.1 |
| C15 | 536.2 | 538.8 | 534.1 | 4.6 | 2.3 | 2.9 |
| C16 | 540.9 | 543.3 | 539.7 | 3.5 | 1.6 | 2 |
| C17 | 537.7 | 541.2 | 535.4 | 5.7 | 2.5 | 3.1 |
| C18 | 537.1 | 539.1 | 535.2 | 3.9 | 1.5 | 1.9 |
| C19 | 535.8 | 539.5 | 533.2 | 6.3 | 3 | 3.7 |
| All Data | 487.5 | 543.3 | 313.7 | 229.6 | 59.8 | 117.1 |

## Appendix E: Processing Data and Calculations (Cont'd)

| Oxide Thickness [nm] STEP 18 | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | | | | AVG | Range |
| C1 | 514.77 | 524.33 | 518.03 | 501.73 | 493.59 | 510.49 | 30.74 |
| C3 | 576.28 | 582.19 | 591.25 | 578.47 | 566.99 | 579.036 | 24.26 |
| C4 | 600.79 | 599.15 | 607.35 | 598.31 | 587.46 | 598.612 | 19.89 |
| C5 | 619.16 | 613.61 | 623.68 | 626.3 | 621.73 | 620.896 | 12.69 |
| C7 | 345.46 | 661.63 | 342.3 | 337.43 | 522.07 | 441.778 | 324.2 |
| C8 | 258.45 | 243.37 | 248.24 | 243.63 | 246.85 | 248.108 | 15.08 |
| c9 | 246.63 | 236.39 | 235.22 | 236.84 | 235.28 | 238.072 | 11.41 |
| c12 | 87.33 | 84.12 | 87.82 | 90.24 | 86.39 | 87.18 | 6.12 |
| c13 | 89.12 | 86.08 | 91.13 | 90.38 | 84.8 | 88.302 | 6.33 |
| c15 | 237.18 | 231.66 | 225.35 | 226.25 | 230.98 | 230.284 | 11.83 |
| c16 | 212.69 | 210.8 | 210.19 | 211.33 | 210.55 | 211.112 | 2.5 |
| c17 | 88.52 | 86.73 | 88.54 | 89.28 | 87.61 | 88.136 | 2.55 |
| c18 | 49.35 | 50.84 | 50.37 | 49.72 | 49.68 | 49.992 | 1.49 |
| c19 | 85.05 | 84.01 | 85.14 | 85.92 | 84.17 | 84.858 | 1.91 |
| D1 | 679.42 | 662.83 | 664.71 | 672.08 | 666.53 | 669.114 | 16.59 |
| D2 | 706.08 | 686.21 | 691.52 | 695.25 | 692.16 | 694.244 | 19.87 |
| D3 | 710.1 | 681.55 | 700.21 | 705.96 | 700.49 | 699.662 | 28.55 |
| D4 | 679.6 | 666.49 | 671.44 | 670.57 | 657.4 | 669.1 | 22.2 |

## Appendix E: Processing Data and Calculations (Cont'd)

| Oxide Thickness Measurements [nm] STEP 25 | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | | | | AVG | Range |
| C3 | 449.16 | 448.29 | 448.3 | 455.51 | 454.53 | 451.158 | 7.22 |
| C4 | 441.6 | 441.5 | 440.95 | 447.7 | 447.29 | 443.808 | 6.75 |
| C5 | 439.61 | 438.38 | 438.76 | 448.31 | 446 | 442.212 | 9.93 |
| C6 | 546.44 | 543.35 | 544.82 | 557.85 | 555.11 | 549.514 | 14.5 |
| C9 | 546.44 | 543.35 | 544.82 | 557.85 | 555.11 | 549.514 | 14.5 |
| c10 | 440.32 | 437.99 | 438.81 | 448.48 | 449.14 | 442.948 | 11.15 |
| D1 | 429.76 | 429.59 | 431.68 | 438.43 | 433.53 | 432.598 | 8.84 |
| D2 | 418.98 | 418.61 | 420.2 | 426.34 | 423.69 | 421.564 | 7.73 |
| D3 | 413.96 | 412.81 | 414.6 | 418.81 | 417.4 | 415.516 | 6 |
| D4 | 407.17 | 405.46 | 407.93 | 414.05 | 413.14 | 409.55 | 8.59 |
| C17 | 321.54 | 331.36 | 338.88 | 351.01 | 346.61 | 337.88 | 29.47 |
| C18 | 283.03 | 289.1 | 299.64 | 315.02 | 313.6 | 300.078 | 31.99 |
| C19 | 263.12 | 258.86 | 283.91 | 281.84 | 265.51 | 270.648 | 25.05 |

## Appendix E: Processing Data and Calculations (Cont'd)

| Oxide Thickness [nm] STEP 38 | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | | | | AVG | Range |
| C1 | 654.28 | 617.53 | 612.49 | 604.76 | 608.23 | 619.458 | 49.52 |
| C4 | 620.46 | 591.33 | 589.84 | 594.33 | 588.62 | 596.916 | 31.84 |
| C5 | 674.16 | 622.81 | 623.26 | 653.57 | 653.63 | 645.486 | 51.35 |
| C10 | 483.99 | 439.42 | 445.62 | 476.02 | 474.35 | 463.88 | 44.57 |
| C11 | 615.02 | 566.35 | 542.34 | 549.97 | 547.22 | 564.18 | 72.68 |
| C15 | 278.06 | 277.21 | 306 | 287.68 | 280.8 | 285.95 | 28.79 |
| C16 | 679.8 | 662.52 | 649.53 | 634.12 | 624.4 | 650.074 | 55.4 |
| C17 | 339.21 | 350.87 | 358.88 | 360.57 | 360.67 | 354.04 | 21.46 |
| C18 | 301.08 | 313.81 | 337.07 | 326.36 | 320.78 | 319.82 | 35.99 |
| C19 | 279.75 | 275.66 | 301.12 | 290.5 | 283.85 | 286.176 | 25.46 |
| D1 | 648.37 | 607.84 | 544.07 | 563.22 | | 590.875 | 104.3 |
| D2 | 612.24 | 608.53 | 579.72 | 543.44 | 543.12 | 577.41 | 69.12 |
| D3 | 659.51 | 612.09 | 626.37 | 603.82 | 608.55 | 622.068 | 55.69 |
| D4 | 629.55 | 599.82 | 596.01 | 556.18 | 576.61 | 591.634 | 73.37 |

## Appendix E: Processing Data and Calculations (Cont'd)

| Oxide Thickness [nm] STEP 48 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | average | stdev | range |
| D1 | 785.65 | 773.00 | 769.35 | 765.19 | 758.18 | 770.274 | 10.20806 | 27.47 |
| D2 | 755.27 | 762.86 | 757.83 | 746.53 | 743.47 | 753.192 | 8.034284 | 19.39 |
| D3 | 775.01 | 759.89 | 753.67 | 740.95 | 743.35 | 754.574 | 13.76861 | 34.06 |
| D4 | 739.22 | 740.78 | 740.36 | 725.01 | 725.32 | 734.138 | 8.211785 | 15.77 |
| C1 | 629.75 | 646.58 | 643.19 | 630.41 | 625.76 | 635.138 | 9.15267 | 20.82 |
| C4 | 728.72 | 730.75 | 729.59 | 715.13 | 718.88 | 724.614 | 7.108012 | 15.62 |
| C5 | 686.74 | 685.71 | 679.82 | 662.87 | 659.56 | 674.94 | 12.85765 | 27.18 |
| C14 | 552.21 | 581.67 | 595.07 | 561.28 | 575.26 | 573.098 | 16.85894 | 42.86 |
| C15 | 813.10 | 817.34 | 815.53 | 814.99 | 815.78 | 815.348 | 1.53048 | 4.24 |
| C16 | 874.92 | 872.15 | 860.14 | 832.83 | 828.06 | 853.62 | 21.93798 | 46.86 |
| C17 | 766.77 | 769.36 | 770.53 | 769.54 | 770.48 | 769.336 | 1.529781 | 3.76 |
| C18 | 771.48 | 774.32 | 773.66 | 773.32 | 774.77 | 773.51 | 1.267202 | 3.29 |
| C19 | 777.09 | 779.85 | 781.61 | 780.73 | 779.23 | 779.702 | 1.714969 | 4.52 |

## Appendix E: Processing Data and Calculations (Cont'd)

Oxide Thickness [nm]

| Furnace Position | | M1 | M2 | M3 | M4 | M5 | Average | |
|---|---|---|---|---|---|---|---|---|
| 1 (Front) | C1 | 321.98 | 313.72 | 337.29 | 334.28 | 331.78 | 327.81 | 12.1 |
| 2 | C2 | 348.32 | 342.28 | 363.79 | 377.16 | 365.37 | 359.384 | 17.4 |
| 3 | C3 | 389.71 | 387.07 | 395.66 | 400.48 | 396.49 | 393.882 | 6.7 |
| 4 | C4 | 414.74 | 412.72 | 423.05 | 430.85 | 429.34 | 422.14 | 10.2 |
| 5 | C5 | 435.09 | 437.41 | 449.91 | 449.62 | 438.16 | 442.038 | 8.9 |
| 6 | C6 | 454.15 | 454.1 | 463.39 | 468.84 | 459.83 | 460.062 | 7.8 |
| 7 | C7 | 468.61 | 464.25 | 469.51 | 473.88 | 472.82 | 469.814 | 4.7 |
| 8 | C8 | 477.4 | 473.88 | 477.92 | 479.51 | 480.18 | 477.778 | 3 |
| 9 | C9 | 485.77 | 487.34 | 486.56 | 491.95 | 494.17 | 489.158 | 4.6 |
| 10 | C10 | 503.65 | 503.93 | 504.12 | 508.01 | 509.34 | 505.81 | 3.3 |
| 11 | D1 | 501.04 | 502.26 | 501.93 | 504.15 | 512.52 | 504.38 | 5.8 |
| 12 | D2 | 504.48 | 505.6 | 506.48 | 512.15 | 508.57 | 507.456 | 3.8 |
| 13 | D3 | 512.74 | 513.38 | 512.53 | 515.98 | 516.22 | 514.17 | 2.2 |
| 14 | D4 | 517.92 | 518.91 | 518.41 | 524.67 | 524.82 | 520.946 | 4.3 |
| 15 | C11 | 527.43 | 527.19 | 528.06 | 531.98 | 531.72 | 529.276 | 2.9 |
| 16 | C12 | 528.39 | 530.18 | 528.86 | 532.89 | 532.89 | 530.642 | 2.7 |
| 17 | C13 | 528.88 | 528.99 | 529.74 | 533.41 | 532.13 | 530.63 | 2.5 |
| 18 | C14 | 537.98 | 538.26 | 536.04 | 539.88 | 540.37 | 538.506 | 2.1 |
| 19 | C15 | 534.4 | 534.92 | 534.1 | 538.75 | 538.69 | 536.172 | 2.9 |
| 20 | C16 | 539.77 | 539.75 | 539.74 | 541.95 | 543.29 | 540.9 | 2 |
| 21 | C17 | 536.98 | 535.44 | 535.54 | 541.16 | 539.44 | 537.712 | 3.1 |
| 22 | C18 | 536.75 | 536.49 | 535.21 | 538.13 | 539.09 | 537.134 | 1.9 |
| 23 | C19 | 534.06 | 533.8 | 533.15 | 538.68 | 539.47 | 535.832 | 3.7 |
| | | | | | | 0 | 572.4 | 500 |

## Appendix E: Processing Data and Calculations (Cont'd)

Sheet resistance

| | Voltage Measurement [mV] | | | | | |
|---|---|---|---|---|---|---|
| Wafer | Average | Max | Min | Range (Max-Min) | Std. Dev | Uncertainty |
| D1 | 494 | 515 | 481 | 34 | 14 | 17 |
| D2 | 420 | 435 | 404 | 31 | 14 | 17 |
| D3 | 415 | 426 | 399 | 27 | 13 | 16 |
| D4 | 425 | 447 | 402 | 45 | 21 | 26 |
| C1 | 458 | 465 | 452 | 13 | 5 | 6 |
| C2 | 337 | 347 | 314 | 33 | 13 | 16 |
| C3 | 508 | 526 | 475 | 51 | 20 | 25 |
| C4 | 478 | 485 | 471 | 14 | 5 | 6 |
| C5 | 446 | 456 | 431 | 25 | 10 | 12 |
| C6 | 475 | 485 | 452 | 33 | 13 | 16 |
| C7 | 455 | 465 | 445 | 20 | 7 | 9 |
| C8 | 321 | 327 | 315 | 12 | 4 | 5 |
| C9 | 432 | 438 | 419 | 19 | 8 | 9 |
| C10 | 468 | 478 | 458 | 20 | 9 | 11 |
| C11 | 466 | 478 | 450 | 28 | 11 | 14 |
| C12 | 404 | 412 | 388 | 24 | 10 | 12 |
| C13 | 426 | 438 | 417 | 21 | 8 | 10 |
| C14 | 482 | 491 | 473 | 18 | 7 | 9 |
| C15 | 448 | 459 | 432 | 27 | 11 | 14 |
| C16 | 456 | 462 | 445 | 17 | 8 | 9 |
| C17 | 463 | 469 | 459 | 10 | 4 | 5 |
| C18 | 422 | 428 | 416 | 12 | 5 | 6 |
| C19 | 428 | 429 | 426 | 3 | 1 | 2 |
| All | 440 | 526 | 314 | 212 | 44 | 0 |

## Appendix E: Processing Data and Calculations (Cont'd)

Step 20 Sheet resistance

| | Wafer | Measured Values [mV] | | | | | |
|---|---|---|---|---|---|---|---|
| | Location | 1 | 2 | 3 | 4 | 5 | avg |
| Current (mA) | | | | | | | |
| 1 | C-8 | 1.972 | 1.928 | 1.952 | 1.986 | 1.903 | 1.9482 |
| 1 | C-1 | 43.4 | 43.7 | 45.2 | 44.5 | 42.7 | 43.9 |
| 1 | C-3 | 36.3 | 46.8 | 45 | 37 | 42.5 | 41.52 |
| 1 | C-10 | Measured Only to Confirm Accuracy | | | | | |
| 1 | C-9 | 1.655 | 1.685 | 1.64 | 1.607 | 1.671 | 1.6516 |
| 1 | C-4 | 41.9 | 44.85 | 46.67 | 43.34 | 42.7 | 43.892 |
| 1 | C-5 | 39.6 | 39.12 | 38.5 | 39.2 | 40.89 | 39.462 |
| 1 | C-7 | 40.9 | 40.6 | 40.8 | 39.2 | 1.99 | 32.698 |
| 1 | C-15 | 1.646 | 1.681 | 1.693 | 1.618 | 1.612 | 1.65 |
| 1 | C-16 | 1.581 | 1.645 | 1.588 | 1.549 | 1.593 | 1.5912 |
| 1 | D-1 | 43.2 | 40.02 | 39.7 | 39.21 | 35.9 | 39.606 |
| 1 | D-2 | 38.6 | 49.7 | 36.8 | 37.5 | 55.2 | 43.56 |
| 1 | D-3 | 33.9 | 57.02 | 33.2 | 33.1 | 38.4 | 39.124 |
| 1 | D-4 | 36.2 | 30.7 | 32.9 | 39 | 38.5 | 35.46 |

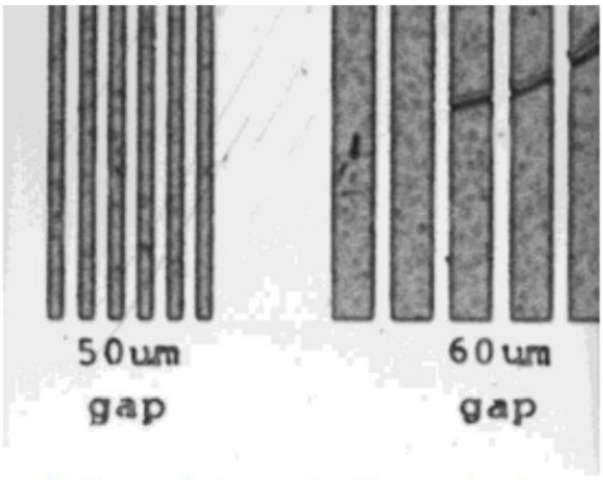
## Appendix E: Processing Data and Calculations (Cont'd)

Step 40 Sheet resistance

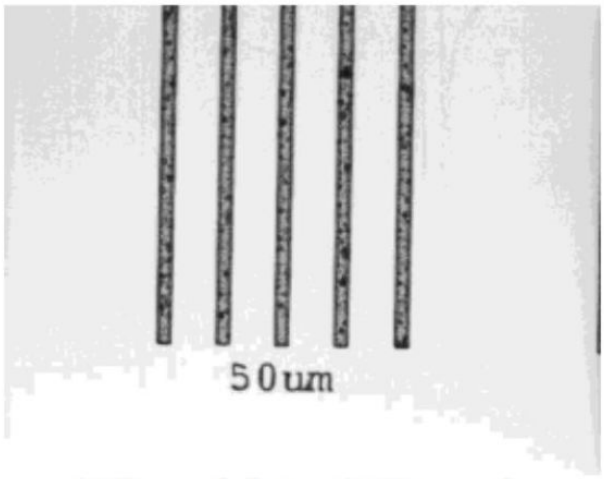
| | 1 | 2 | 3 | 4 | 5 | AVG |
|---|---|---|---|---|---|---|
| C11 | 1.783 | 1.998 | 2.076 | 2.42 | 2.318 | 2.119 |
| C15 | 1.805 | 1.825 | 1.822 | 1.751 | 1.76 | 1.7926 |
| D1 | 6.62 | 7.75 | 5.2 | 37.9 | 40.1 | 19.514 |
| D2 | 6.13 | 9.19 | 14.69 | 16.1 | 35.8 | 16.382 |
| D3 | 1.3 | 10.27 | 40.5 | 19.42 | 5.65 | 15.428 |
| D4 | 3.662 | 5.59 | 0.752 | 24.5 | 32.24 | 13.3488 |
| C4 | 21.81 | 20.85 | 15.5 | 19.4 | 18.3 | 19.172 |
| C5 | 1.3 | 5.166 | 2.62 | 17.6 | 19.25 | 9.1872 |

# Appendix F: Processing Images

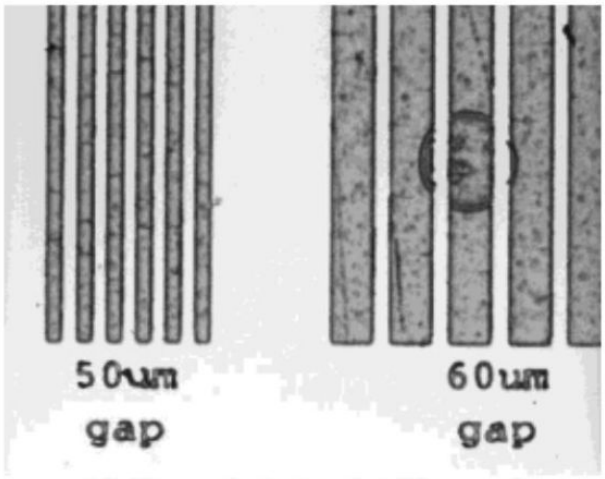
(a) Mask




(b) Exposed photoresist 25 seconds; chosen exposure time




(c) Exposed photoresist 20 seconds; underexposed




(d) Exposed photoresist 30 seconds; overexposed

# Appendix G: Diode Data

| C5 | | C5 | | C5 | | C5 | | D4 | | D4 | | D4 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| row 5 column 1 | | row 5 column 1 | | row 5 column 1 | | row 5 column 1 | | row 8 column 5 | | row 5 column 1 | | row 5 column 9 | |
| C5 Die 51 Diode 45 | | C5 Die 51 Diode 11 | | C5 Die 51 Diode 65 | | C5 Die 51 Diode 55 | | D4 Die 85 Diode 33 | | D4 Die 51 Diode 33 | | D4 Die 59 Diode 33 | |
| voltage | current | voltage | current | voltage | current | voltage | current | 4.25 | 240 | -2.75 | -133 | 2.75 | 85 |
| -5 | -119 | -5 | -193 | | | -5 | -262 | 4 | 222 | -3 | -146 | 3 | 99.4 |
| -4.5 | -106 | -4.5 | -172 | | | -4.5 | -234 | 3.75 | 174 | -3.5 | -185 | 3.25 | 121 |
| -4 | -88.2 | -4 | -145 | | | -4 | -202 | 3.5 | 140 | -3.25 | -167 | 3.5 | 137 |
| -3.5 | -70.3 | -3.5 | -121 | | | -3.5 | -171 | 3.25 | 129 | -2 | -82 | 3.75 | 153 |
| -3 | -55.9 | -3 | -91.3 | -5 | -325 | -3 | -138 | 3 | 108 | -1.5 | -53 | 4 | 168 |
| -2.5 | -41.6 | -2.5 | -66.2 | -4 | -252 | -2.5 | -112 | 2.75 | 97 | -1 | -31 | 4.5 | 203 |
| -2 | -27.6 | -2 | -45.5 | -3.5 | -213 | -2 | -77.8 | 2.5 | 86 | -0.5 | -7.7 | 5 | 238 |
| -1.5 | -14.5 | -1.5 | -29 | -3 | -182 | -1.5 | -31.6 | 2.25 | 75.6 | -0.6 | -9.8 | -5 | -216 |
| -0.8 | -3.9 | -0.8 | -7.62 | -2.2 | -120 | -0.8 | -25.3 | -2.5 | -73 | -0.4 | -5.77 | -4.5 | -184 |
| -0.5 | -1.26 | -0.5 | -3.88 | -1.5 | -72.2 | -0.5 | -10.8 | -2.75 | -86 | -0.3 | -4.18 | -4.25 | -169 |
| 0 | -0.0155 | 0 | -0.029 | -1 | -41.9 | 0 | -0.199 | -3 | -100 | -0.7 | -15.9 | -4 | -154 |
| 0 | 0 | 0 | 0.009 | 0 | -0.19 | 0 | 0.016 | -3.25 | -116 | 0.7 | 19.2 | -3.5 | -124 |
| 0.5 | 1.03 | 0.5 | 1.24 | 0 | 0.071 | 0.5 | 4.33 | -3.5 | -124 | 0.5 | 9.05 | -2.75 | -78 |
| 0.8 | 3.5 | 0.8 | 4.14 | 1 | 29.1 | 0.8 | 11.6 | -3.75 | | 0.3 | 4.69 | -2.25 | -54 |
| 1.5 | 15.5 | 1.5 | 22.4 | 1.5 | 59.4 | 1.5 | 16.5 | -4 | | 1 | 33.06 | -1.75 | -33 |
| 2 | 27.6 | 2 | 39.8 | 2.2 | 105 | 2 | 44.5 | | | 1.5 | 60.2 | -1 | -8.5 |
| 2.5 | 42.9 | 2.5 | 60.6 | 3 | 159 | 2.5 | 68.9 | | | 1.74 | 13.6 | -0.75 | -4.9 |
| 3 | 56.7 | 3 | 89.8 | 3.5 | 197 | 3 | 100 | | | 2 | 88.9 | -0.5 | -2.2 |
| 3.5 | 73.1 | 3.5 | 115.7 | 4 | 238 | 3.5 | 149 | | | 1.69 | 70.7 | -0.42 | -1.7 |
| 4 | 93.9 | 4 | 143 | 4.9 | 305 | 4 | 192 | | | 1.4 | 54.2 | -0.6 | -3.28 |
| 4.5 | 110.8 | 4.5 | 176 | | | 4.5 | 233 | | | 1.6 | 65.4 | | |
| 5 | 138 | 5 | 208 | | | 5 | 263 | | | 2 | 90.5 | | |

# Appendix H: Resistor Data

As the data for the resistor spans many pages, the data may be provided upon request.

| A | Ω | | |
|---|---|---|---|
| | average | stdev | uncertainty of mean |
| M | 22 | 18 | 9.873 |
| P | 2,482 | 2,209 | 648.566 |
| N | 1,369,072 | 2,010,186 | 590212.844 |

| B | Ω | | |
|---|---|---|---|
| | average | stdev | uncertainty of mean |
| M | 26.55 | 3.34 | 5.306993616 |
| P | 3,364 | 3,138 | 1391.209136 |
| N | 1,144,152 | 1,556,028 | 657052.9002 |

| F | Ω | | |
|---|---|---|---|
| | average | stdev | uncertainty of mean |
| M | 73.54 | 27.86 | 2.14E+01 |
| P | 1,032,365 | 3,296,813 | 8.24E+05 |
| N | 10,248,943 | 60,049,201 | 14999844.17 |